WIRELESS EMBEDDED TEST FOR RF/MICROWAVE IC

By

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WIRELESS EMBEDDED TEST FOR RF/MICROWAVE IC

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The explosive growth of RF/Microwave IC industry has made the testing of RF/Microwave applications very challenging, particularly under the constraints of high quality and low price. Embedded test is a potential solution to face the challenges posed to RF/Microwave IC test, in which low-cost testers, already on the factory floor, can be applied to perform RF/Microwave ICs testing with additional design for test (DFT) circuitry integrated with the IC under test, instead of costly advanced ATE system with RF functions.

The fundamental idea is to move very high-speed test functions on-chip, thus reducing the requirement and the cost of the external ATE. This move, however, is not that simple, and still in the development stage.

The basis of the proposed wireless embedded test is an off-wafer (chip) tester plus some test circuitry integrated with the device-under-test (DUT). The on-wafer (chip) test circuit receives a signal from the external signal source, modifies it into a suitable test stimulus for the DUT, and then extracts the useful information from the response of the

DUT into baseband signals, which are finally transmitted back to the external tester. The external tester and antenna are needed for sending the initial RF signals without any physical interconnection to the DUT and receiving the low-speed test response from the DUT by low-frequency wire connections. Thereby, the necessary on-chip components of the proposed embedded test are an antenna, power and high frequency rectification and sensing circuitry.

First, the design and implementation of an RF RMS detector for embedded test is presented, which is based on a bipolar translinear design methodology. Then single-layer and multi-layer on-chip antennas with different lengths are developed, the performance of which will be compared with the measurement results. Next, CMOS frequency dividers are reviewed, including theoretical analysis of injection locking performance and designs of injection-locking frequency dividers and flip-flop-based frequency divider at 12 GHz and 24 GHz. With the designed on-chip antenna and frequency dividers, a simple microwave test source is built. Finally, the application of the test source is studied and a wireless embedded test scheme for LNA is proposed.

CHAPTER 1
INTRODUCTION

1.1 Background of RF/Microwave IC Test

Usually RF/Microwave measurements can be categorized into two classes, scalar tests and vector tests. Scalar tests are concerned with measurement of signal amplitudes, but not phase. Examples of scalar tests are gain, spurious and harmonic tests, linearity, and noise figure. In contrast, vector tests involve measurement of both magnitude and phase. Examples include scattering or S-parameters, voltage standing wave ratio (VSWR) and group delay. Some examples are shown in figure 1-1.

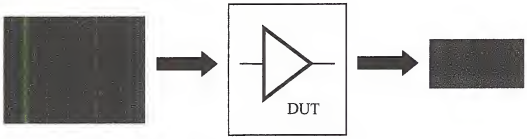


Figure 1-1. Conventional RF IC testing

Before 1983, high-speed, integrated circuit (IC) designers could only speculate as to why a particular design worked. The true electrical performance of these tiny microwave circuits was impossible to measure at the wafer level. With the development of high-performance and high-frequency on-wafer probes and probe stations, design engineers could test and characterize their circuits on-wafer, before the ICs were diced and packaged. Since then, RF measurement systems evolved from rack-and-stack systems to extremely complex, million dollar Automatic Test Equipment (ATE). RF ATE

is actually several RF instruments rolled into one--signal generators, power meters, spectrum and network analyzers and noise figure meters, that can provide a much higher throughput capability than traditional rack-and-stack systems. But on-wafer testing in this way is not only expensive but also time-consuming.

Since the early days of silicon, wafer-level testing has been used to prune away catastrophically defective dies before packaging. Since all dies that pass the wafer-level testing are again tested thoroughly after packaging, the cost of wafer-level testing needs to be extremely low. The high cost of RF testers coupled with the difficulty of measuring RF signals has limited wafer-level testing to digital circuits only. Thus, during wafer-level testing, the RF path is completely bypassed.

With improvements in manufacturing technology, and relaxed performance requirements of some application domains, leading to easier design processes, the cost of manufacturing RF dies has appreciably reduced. However, each manufactured die which passes the wafer-level digital testing, and whether or not there is any defect in its RF path, still needs to be packaged and fully tested, the cost of which has not reduced at the same rate as design and manufacturing. As the packaging cost becomes an appreciable component of the overall cost and the yields are lower as a result of increased IC complexities, bypassing the RF path during wafer-level testing proves to be an inefficient method in terms of the overall cost. Plus, there are new configurations of RF/mixed-signal IC system in a package which need to be tested prior to assembly. However, utilization of existed RF testing methods on wafer-level testing faces many challenges as well.

1.2 Challenges to RF/Microwave IC Test

Over the past decade, it has been observed that the radio frequency (RF) wireless market expanded to unimaginable size. Devices such as pagers, cellular and cordless phones, cable modems, and RF ID tags are rapidly penetrating all aspects of our lives, evolving from luxury items to indispensable tools. Meanwhile, due to the increasing demands for broadband wireless communication, higher frequency bands such as microwave and millimeter-wave where there is sufficient spectrum are of growing interest. The recent rapid development of Si-based CMOS devices makes it possible to implement low cost and high integration circuits at such high frequencies [YU04, Gua04]. Simultaneously, the integration density and complexity of these devices increase with customers' demands in functionality.

This explosive growth of wireless communication industry has made the testing of RF/Microwave applications very challenging, particularly under the constraints of high quality and low price.

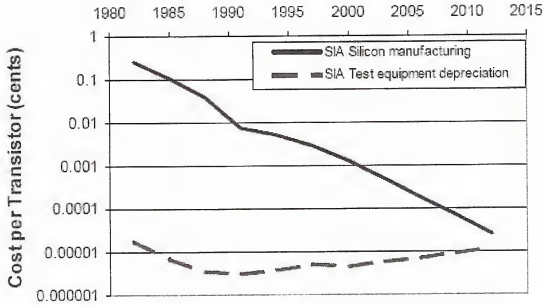


Figure 1-2. Moore's law for test: fab .vs. test capital

The dominant challenge is testing cost. In the past, RF/Microwave applications have imposed stringent performance requirements on the design, manufacturing and testing, which led to high overall costs. And despite the high production cost, high market prices could still provide adequate profitability for them. However, with increasing competitions in traditional applications, such as cellular phones, and emerging application domains, such as sensor networks, profit margins are decreasing and the cost pressure becomes prohibitive. And the cost dynamics for ICs are also changing. Before, RF design and silicon manufacturing have contributed the highest components to the total cost, thus drawing little attention to testing. With recent improvements in manufacturing technology, and relaxed performance requirements of some application domains, leading to an easier design process, the cost of manufacturing RF dies has appreciably reduced. It can be seen that the manufacturing cost per transistor indeed follows Moore's Law, which reduces the cost per IC even as functionality and performance increases, while test costs don't scale with Moore's Law, therefore becoming a bigger factor in the total manufacturing cost of a chip. Figure 1-2 shows a plot extrapolated from the 2001 International Technology Roadmap for Semiconductors (ITRS) [ITR01]. It depicts the capital costs for chip fabrication versus the capital costs for manufacturing test, normalized per transistor. The top curve shows the consistent reduction in chip fabrication cost per transistor that in turn drives the continued expansion and evolution of the semiconductor business. The bottom curve indicates capital expenses for IC test have been essentially flat per transistor. But this does not mean IC test really has been standing still for the last 20 years, rather the historical test trend exhibits the tremendous amount of effort and technology in test to keep up with the continued increases in IC device

performance and complexity. Even so, the test capital per transistor still trends to rise as in the plot. If not addressed, the data in Figure 1-1 would project the industry would reach a point in several years where the general cost of testing ICs exceeds the cost of fabricating them.

Associated with testing cost is testing time. Nowadays the commercial wireless industry demands extremely low cost RF components, and a key contributor to the cost of RF ICs has been the test time per part. For an ATE system, total test time includes Tester Capability/Speed (Electrical Test Time), Handler/Tester/Controller Communications Time, Handler Capability and Index Time of Handler. As an example, figure 1-3 shows the relationships between test cost and test time; the information source is from IBM test development group [IBM02]. The left plot illustrates the test cost for a $2M tester and the right plot illustrates the test cost for a $100K tester. Both plots show test cost/part is almost entirely a function of test time.

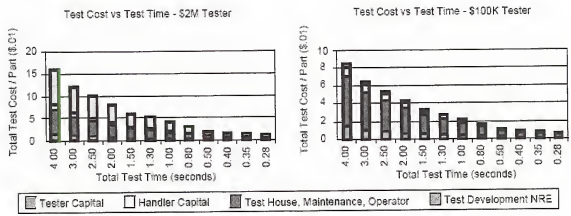


Figure 1-3. Cost contributors to testing a part for various test times

Another challenge is visibility and accessibility in the testing of ICs. Increasing wafer size with decreasing feature size, coupled with more complex fabrication processes, causes the characteristics of the devices-under-test (DUTs) immeasurable or

even inaccessible using existing testing methods, which is especially significant for RF/Microwave ICs. For instance, at frequencies above 5 GHz, it is hard to tell the value of the signal injected into the DUT from external ATE. At the same time, as density and complexity of circuits increases, the number of input/output pins remains relatively constant, thus the need for added testing pads and increased placement precision of testing probes is more and more demanding and expensive.

In addition, the fault model paradigm, extremely successful in digital tests, has not been standardized for analog RF tests and the fall-back position is still specification-based tests, which were developed for stand-alone components and do not really fit the system test protocols. New paradigms are being investigated but encounter strong resistance in applications since these new techniques have not been correlated to existing techniques to convince the industry of the test robustness and quality.

Clearly, it is important to look for innovative ways to circumvent these challenges and make test techniques catch up the pace of RF/Microwave ICs' performance.

1.3 Potential Solutions

While the testing requirements and procedures for various RF/Microwave ICs differ widely, all are tested at very high frequencies, typically at 900 MHz or higher. Potential solutions to response the challenges to RF/Microwave ICs' testing can be categorized as follows:

Test cost and time reduction for RF/Microwave ICs can fall into three techniques: test less, test earlier and test faster [Eri98]. Test less exploits redundancy among the tests, like between the wafer level tests and final tests. With test earlier, package scrap is reduced by performing as many tests on-wafer as possible. Final test is still necessary, but

often limited to continuity tests for high yield production lines. Test faster involves the use of test parallelism or high-throughput testers.

To address the limitation of visibility and accessibility in the testing of ICs, the simplest approach is to use a multiplexer to add test points at the I/O of the analog subsystem to be tested. This methodology is originally proposed by Wagner [Wag88], and is still commonly used in industry. This technique permits the monitoring of one signal at a time but degrades the test accuracy as the number of test points is increased and at higher speed operation of the DUT because of the capacitive load of the multiplexers

IEEE1149.1 (JTAG) boundary-scan standard provides an effective means for test-access to internal modules of the DUT for testing static faults in digital ICs. Its JTAG counter part in mixed-signal testing, the IEEE P1149.4 standard [IEEE99], extended to cover RF/Microwave devices has been discussed in many different publications [Heu99, Alt03]. In these papers, the boundary-scan standard provides only an indirect testability to the RF devices, which limits the resolution of RF diagnostics. To provide a structural test solution for RF circuits and increase the resolution of RF diagnostics, the boundary scan standard should be directly implemented on RF input and output ports. However, there are many difficulties to perform boundary-scan tests on RF pins. The main reason is that adding additional test circuitry to the parasitic sensitive RF lines is not trivial and can easily degrade the RF performance of the RFICs. Though some improvements have been made [Hua04], more study is needed for the on-chip extension of the boundary-scan standard.

Fault-based test development approaches have flourished for years, mostly from academic publications. The extension of digital fault models to analog fault models has created several new fault classes [Som97], most notably the catastrophic fault models and the parametric fault models. Test techniques based on these models have been developed and are strongly biased toward the re-use of existing tests and seek to validate them based on a fault coverage measure defined and computed based on a selected fault model. These developments to date have not been in frequent use by industry since there is no agreement on an adequacy and usefulness of fault models. The correlation with specification-based tests, critical to industry acceptance of new techniques, has not been demonstrated and viable analog fault models have yet to be discovered.

Another potential solution is the use of embedded test, in which low-cost testers can be applied to perform RF/Microwave ICs testing instead of costly advanced ATE system with RF functions. Actually, embedded test is comprised of two distinct test approaches: external ATE and conventional DFT. This test integration facilitates the chip, board and system level test, diagnosis, debug and repair. Typically, embedded test is implemented in two components [Zor02]: user configurable test IP (intellectual property) in the form of design objects delivered as Register Transfer Level (RTL) soft cores; and a suite of test automation tools to automate generating, integrating, analyzing, and verifying test and diagnostic patterns. The fundamental approach is to move very high-speed test functions on-chip, thus reducing the requirement on and the cost of the external test. This move, however, is not that simple, and still in the development stage.

The use of embedded test can improve circuit controllability and enhance circuit observability. Given reliable embedded test, the time spent in ATE can be reduced,

thereby lowering the cost per chip. With embedded test, comprehensive fault coverage with minimal external intervention is enabled – a benefit that extends not only to production test but also to ongoing field maintenance. During production, an ATE can activate the test sequence and read the pass or fail result. For device debug, design tools interact with the DUT to diagnose the failure quickly. The bigger advantage is that circuit functionality can be tested and validated throughout the lifetime of the device. This includes debugging remote systems that are in the field.

1.4 Overview of Dissertation

This dissertation concentrates on the design issues of various components in a proposed wireless RF/Microwave IC embedded test vehicle, as well as the evaluation of the system feasibility, which serves as the first step for implementing future low-cost RF/Microwave test wirelessly. The graphic overview of the whole work is shown in figure 1-4.

In chapter 2, some features and trends of current embedded test are first introduced, followed by several example RF/Microwave IC test architectures. A new wireless RF/Microwave IC embedded test vehicle is then proposed, which include an on-chip microwave antenna, analog/digital dividers and RF detectors. As an application, the proposed test structure is used to test a low-noise-amplifier (LNA), all of which are integrated on the same chip.

A new RF RMS detector with very wide bandwidth is presented in chapter 3, which is based on the dynamic translinear principle and integrated in a BiCMOS process. The main computation is carried out in the current domain and errors due to finite transistor gain are compensated in a novel circuit structure. Monte Carlo analysis is used to check

the design for the process and mismatch variations. To make the circuit suitable for voltage processing, both input and output interface circuits are included. Test setup and measurements on a prototype chip demonstrate the practicality of the circuit for on-chip embedded tests.

A critical component of a wireless test system is the antenna, which acts as a receiver of external test signals. The implementations of various-length on-chip zigzag dipole antennas are discussed in the first part of chapter 4. The designed antennas can be considered as transducers between the incoming electromagnetic (EM) wave and the current and voltage within the subsequent circuitry. Since they are integrated with other circuits on the same chip and for the purpose of embedded test, these antennas should be area-efficient, and meanwhile keep the antenna gain maximized. Both simulation results with EM simulation tool HFSS and measured results of on-chip antennas are evaluated and demonstrate the plausibility of small on-chip antennas as a receiver for external test signals.

The second part of Chapter 4 demonstrates the designs and measurements for different types of frequency dividers. The analog dividers are designed using the phenomena of injection pulling and locking in an LC-based oscillator, so-called ILFD. Three ILFDs were implemented with 0.18um technology. Two of them utilize all NMOS differential LC VCO with indirect injection topology and resonate at 12 GHz and 6GHz respectively. The third one employs CMOS differential LC VCO with direct injection topology, the free running frequency of which is 12 GHz. A CMOS source-coupled logic (SCL) frequency divider is implemented with the same technology, which can operate

within a wider bandwidth than the analog ones. The performance difference on different types of dividers is shown through the simulations of each divider.

The generation of an on-chip RF/Microwave test signal source is developed in chapter 5, which utilizes the on-chip antenna and frequency divider described in the last two chapters. The on-chip passive antenna receives the incoming microwave signal with little distortion and passes the signal into the input of the frequency divider. The frequency divider then divides the frequency of the signal into the desired band. Since the frequency divider is implemented based on the principle of injection locking. The phase noise performance of the generated on-chip signal is comparable to that generated by the external tester. This solves the problem existing in the wired test system that test signals at or above 5 GHz are severely degraded when they are passed onto the DUT from the tester. The future measurement results will prove the realizability of such an on-chip RF/Microwave signal source.

The goal of this work is to demonstrate the operation of RF/Microwave wireless embedded test and evaluate its feasibility. Apart from the generation of on-chip RF/Microwave test signal source, Chapter 5 displays an application of the proposed wireless RF/Microwave embedded test. In this demonstration, an LNA, which is the most common and key component in RF front-end, serves as DUT and is integrated with the embedded test function circuits discussed in the previous chapters. A test signal is injected from the on-chip signal source, and the RF detectors sense the signals from the DUT and output the dc signals to the external low-cost ATE. With this method, the figures of merit characterizing the LNA can be accurately obtained, which include voltage gain, transducer gain, input impedance and noise figure. Compared to

conventional LNA tests, this prototype scheme of LNA embedded self-test is simple and cost-effective. It is worth exploiting further in the future.

Finally, chapter 6 summarizes the overall work in this dissertation and concludes the feasibility of the wireless RF/Microwave embedded test and future work is suggested.

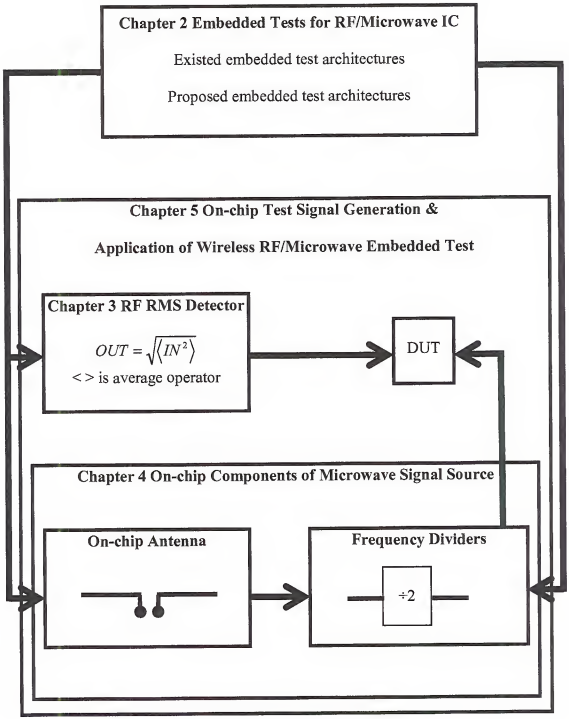


Figure 1-4. Flow chart of dissertation

CHAPTER 2
EMBEDDED TEST FOR RF/MICROWAVE IC

2.1 Introduction

Embedded test as a potential solution to face the challenges posed to RF/Microwave IC test is introduced in chapter 1. Embedded test proposes a flexible paradigm for RF/Microwave test while providing scalability with advances in design. Usually embedded test includes designing test hardware on-chip, supporting the test hardware with design for testability (DFT) features and designing in standard communication protocols that allow an external tester to control the test procedure with low-bandwidth access and hence, lower cost external testers. Recent studies [Dab03, Haf03, Cha04, Eis04 and Sel04] have demonstrated the ability to measure RF/Microwave circuits via compact on-chip test structures and a low-cost external tester.

With a typical RF ATE, which may include functions of DC bias, DC measurement, RF power meter, network analyzer and etc., RF/Microwave test signals are being transported across the package to IC boundary for excitation or measurement. Unfortunately, at frequencies above 5 GHz, signals that pass between the ATE system and the DUT can be significantly degraded. Variability of mechanical pogo-pin placement in the connections to IC packages, load-board signal loss, and package and load-board crosstalk can create large uncertainties in the amount of power delivered from the IC tester into the IC. In the future, required guard-banding for the IC tester signal connection uncertainty may create significant rejection of good ICs during manufacturing test. Finally, the signaling specifications will be increasingly complex and transmitter

output spectral requirements more stringent, which will stretch the manufacturing test development time [Eis04]. An alternative to this approach is to integrate some additional circuitry functioning as RF exciting or measuring with the DUT or reuse some components already available in the DUT. In this way, high frequency communication is constrained on-chip and eliminated between the DUT and the external tester. And instead of a costly RF tester, a low-cost external tester can be employed to monitor low-speed communication taking place between it and the built-in circuitry inside the DUT, as shown in figure 2-1. If the effects of the additional circuitry on the DUT, such as device mismatching, parasitic loading and more area requirement, can be negligible, low-cost RF/Microwave test is plausible.

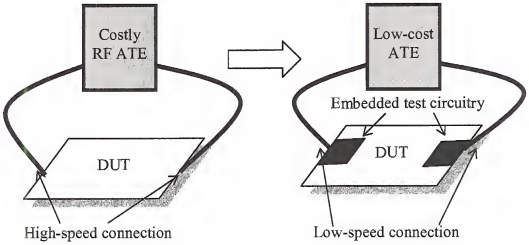


Figure 2-1. Evolution of embedded test

The rest of this chapter is organized as follows: in section 2.2, some recent work on RF embedded test are reviewed, including the trade-offs and design issues of these approaches; section 2.3 describes the proposed wireless RF/Microwave embedded test.

2.2 RF Embedded Test Overview

2.2.1 ADC/DSP-based Approach for RF Embedded Test

Motivated by analog integration trends and the increasing difficulty in transferring test information using a conventional setup, an ADC/DSP-based embedded test is adopted by Hafed and Roberts [Haf03], in which both a waveform generator and a waveform digitizer are integrated in the form of a D/A converter and an A/D converter, respectively. Thereby, test information can be available in the digital domain for further processing on or off the IC.

Figure 2-2 illustrates a block diagram of the components comprising the ADC/DSP-based embedded test. It consists of two one-bit memories (or sequential-registers), some analog structures, and a multi-bit memory for output data storage. The memory on the left part of the figure consists of two bit stream generators, one for ac stimulus generation, and one for dc signal generation. The latter is combined with the analog comparator to perform multi-bit resolution digitization.

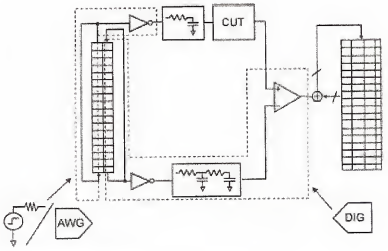


Figure 2-2. ADC/DSP-based embedded test structure

The ac waveform generator synthesizes test frequencies using a short repetitious sequence of digital bits. This sequence is chosen to approximate the output of a 1-bit sigma–delta modulator. Specifically, a finite duration of the output of a software sigma–delta modulator that is driven by a periodic input is captured and periodically repeated on-chip to approximate the infinite-duration sigma–delta modulator output.

On-chip waveform digitization is achieved using the second bit stream generator (the dc generator), a passive on-chip RC filter, and a voltage comparator. Multi-bit digitization using such limited hardware is achieved by making use of the periodicity of the input signal. In this approach, the way the signal is digitized is as follows. All samples of a unit test period are compared to a single quantization level, say 0 V, set by the dc voltage generator. Once all incoming samples are compared to this level, the dc bit stream generator is commanded to increment its output to the next quantization level, and the process repeats. The encoding method used in the dc bit stream generator is also based on approximating sigma–delta modulated streams. Specifically, the one-bit nature of the sigma–delta streams significantly reduces sensitivity to process mismatches and preserves linearity. Similarly, drifts in RC component values do not alter the average output of the filter. It is recognized that temperature as well as aging will affect the proposed circuits in much the same way that they would affect external measurement instruments. Such effects are generally minimized using a controlled test environment and/or calibration.

The capture algorithm relies primarily on the proper synchronization with the excitation system. Such synchronization is achieved in this system, which fixes the stimulus and capture sample rates in order to achieve a coherent measurement setup.

Processing of the comparator output is done using a multi-bit memory (Figure 2-2) that is the same length as the length of the unit test period and that is initialized to zero at the beginning of a measurement run. This memory can be integrated on-chip or in software, depending on the application. For each comparison pass, the bit stream generators continuously circulate their contents to output the analog stimulus and the reference level, respectively. For each circuit response sample, the corresponding memory location is incremented or left unchanged, depending on whether the comparator output (for the current dc level) was 1 or 0. At the end of the digitization process, each memory location will contain an integer count representing the quantization level for the corresponding sample (i.e. a thermometer code).

The benefits from this approach include the elimination of long interconnect problems, less capital cost and high fidelity measurement because of digitalization of test signals. In addition, a memory-based approach allows for faster design times, robustness to process variation, and scalability. But to a large extent, the bandwidth of this test structure is limited by the capability of its A/D and D/A converters.

2.2.2 Loop-back Approach for RF Embedded Test

For wireless communications and portable devices, current test techniques are often based on some kind of loop-back approach, in order to reuse the transmitter or receiver section.

A typical loop-back test block diagram of a present RF transceiver is shown in figure 2-3 [Dab03]. All the functional blocks except of the power amplifier (PA), RF filter and diplexer with antenna are integrated on one chip. To enable the embedded test, the test amplifier (TA) has been added to the chip. With this approach, the on-chip RF

front-end is targeted rather than the complete transceiver, for which a set of detailed tests is prescribed by standards that a vendor must comply with.

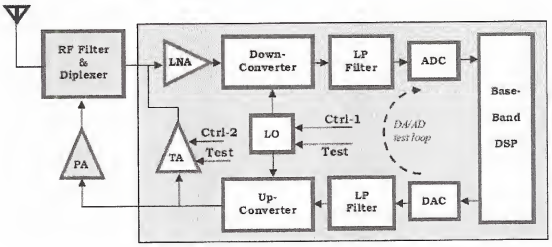


Figure 2-3. Block diagram of loop-back approach for RF embedded test

In the figure, the base-band processor serves both as a stimulus generator and response analyzer. The test loop comprising the transmitter (Tx) and receiver (Rx) path is closed by TA. A possible local test loop aimed at DA/AD converters is marked with the dashed arrow (filters can be included too). This structure requires additional multiplexers, not shown in the figure. It is assumed that testing the DA/AD converters precedes the RF front-end test. The TA is a low power variable gain amplifier, which is powered down in normal operation mode, and should not affect the transceiver performance. The frequency synthesizer (LO) is involved as well, and in test mode it must support Tx to operate at the carrier frequency of the receiver (that might be different from the normal mode).

When the loop-back test targets the receiver blocks, the control path traces through Tx and TA. The frequency synthesizer (LO) is involved as well. The stimulus for testing Rx blocks has three attributes: Base band digital content (pattern), frequency of RF carrier, and RF carrier level. Different functional blocks are involved with those

attributes. When the loop-back test aims at the transmitter blocks, the control path is very short, but the observation path traces through TA and Rx. Also LO is involved. In this case, the carrier level is not the stimulus attribute, but is important to retrieve the response. The distinction between control path and observation path is important during verification of the test stimuli in order to target a faulty block in the loop (fault simulation).

The above loop-back technique makes use of the "duality" present in the transceiver system. The output of a receiver is analyzed by its dual transmitter and vice versa. However, test interconnections require additional components to balance power levels and to overlap the frequency bands of two subsystems. Furthermore, consecutive stages mask fault effects, and during testing, the loop can only be addressed as a whole, hence the fault diagnosis is a hard problem.

2.2.3 Alternate Test Approach for RF Embedded Test

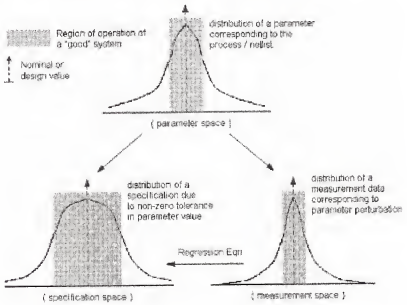


Figure 2-4. Relationship between manufacturing process, DUT specification and test

The basic idea behind alternate test is that the DUT performance is related to (and, in turn, is affected by) process variations, and that it is possible to predict the DUT performance using additional tests that are much "cheaper" to perform than tests that explicitly measure the performance specifications.

As shown in figure 2-4 [Cha04], a mapping function f: M->S can be constructed for the circuit specifications S from all the measurements in the measurement space M using nonlinear statistical multivariate regression. Given the existence of the regression model for S, an unknown specification of a DUT can be predicted from the measured data

The objective of the alternate test methodology is to find a suitable transient test stimulus and to predict circuit specifications accurately from alternate test response. The methods are targeted at low-cost testing of RF front-ends and front-end chips, such as LNAs, power amplifiers, attenuators and mixers. Different type of test stimuli can be used in different cases.

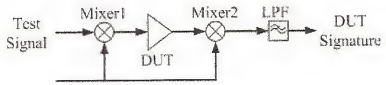


Figure 2-5. Basic alternate test configurations for RF IC

The basic alternate test configuration for testing RF IC is illustrated in figure 2-5. The concepts of modulation and demodulation are applied to translate a transient base band test stimulus to the RF spectrum for applying to the DUT, and the DUT response back to base band signature. The low-cost tester supplies a carefully designed base band test stimulus and the stimulus is then modulated onto a carrier via mixer 1. This

modulated carrier is the test input signal to the DUT. The response of the DUT is demodulated to base band and sent back to the external test. The design of the test stimulus (base band + carrier) is done in such a way that the performance variations in DUT cause significant changes in the response see by the tester.

The main feature of this test approach is that multiple DUT specifications can be measured using a single acquisition and a single test configuration. As testing is performed on a low-cost ATE using an extremely short duration test stimulus, improvement in test throughput and test costs of RF circuits is made possible. But with the need of additional resources, like mixers or A/D converters, area overhead is increased. The quality of RF test stimulus may be degraded because of the modulation and demodulation involved with mixers.

2.3 Proposed Wireless RF/Microwave Embedded Test

2.3.1 Potential Benefits

Given the distances that signals have to travel in a conventional measurement setup, usually in the range of 10 cm ~ 100cm, and at high frequencies, for instance, at 1 GHz, the wavelength of a signal is only 3 mm in air, transmission line theory becomes more effective than lumped-circuit theory in describing the effect of the interconnect between the device under test and the measurement instruments. The issue in high-speed measurement becomes that of interconnect uniformity (matched impedances throughout signal paths). Ensuring that the measurement results exclude the transmission properties of the interconnection is generally rather costly and requires a significant level of effort and expertise. For example, a common approach is to measure the scattering parameters of the interconnection and to formulate mathematical models to decouple the response of

the interconnection from the actual response of the device being measured. Unfortunately, this is becoming extremely cumbersome as test path calibration accuracy is no longer simply determined by the instrument alone but rather by the whole combination of device under test, instrument, and the connection media in between. Embedded test is one way to circumvent this bottleneck of RF/Microwave IC test, in which the external tester controls the generation of on-chip test stimulus by baseband communication and the high frequency response from DUT is converted to baseband signals on-chip and then sent to the external tester. Hence, to handle RF/Microwave test, embedded test still presents the following major challenges:

1) on-chip generation of high-quality and high speed test signals using low-cost hardware;
2) high-speed on-chip response acquisition followed by analysis or response compaction.

Through the discussion of different embedded test structures in section 2.2, it can be seen that to satisfy the above two challenges is still a tough job. With ADC/DSP-based approach, the speed of test stimulus is limited by the capability of mixed-signal circuitry. It is nearly impossible to generate a high-quality and a high speed test signal with a simple area-effective on-chip ADC. Similarly, the compact on-chip modulation and demodulation process in alternate test can not guarantee the quality of signals as well. The loop-back approach is constrained by the type of DUT and can not do fault diagnosis locally. Therefore, the opportunity for a wireless embedded test methodology becomes evident.

As shown in figure 2-6, the basis of the wireless embedded test is an off-wafer (chip) tester plus some test circuitry integrated with the DUT. The on-wafer (chip) test circuit receives a signal from the external signal source, modifies it into a suitable test

stimulus to DUT, and then extracts the useful information from the response of the DUT into baseband signals, which are finally transmitted back to the external tester. The external tester and antenna are needed for sending the initial RF signal without any interconnection to the DUT and receiving the low-speed test response from the DUT by general wired connections. Thereby, the necessary on-chip components of the proposed embedded test are an antenna, power and high frequency rectification and sensing circuitry.

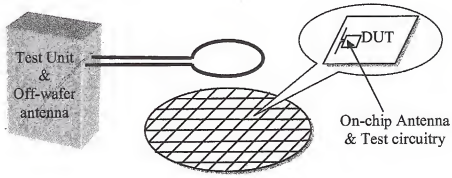


Figure 2-6. Wireless embedded test setup

Compared to other existed RF/Microwave test methods, the potential benefits offered by the proposed wireless embedded test methods are listed as follows:

First, wireless communication provides a short direct connection between a tester and DUTs. This ensures that the measurement results exclude the transmission properties of the interconnection. No matched impedances throughout signal paths need to be considered, hence, no scattering parameters between the tester and the DUT are measured. In addition, usually, as the increasing of the operation frequency, it is harder to make tests with traditional test setups because of signal degradation. But with wireless

technology, somehow, it is easier to transmit the test signal with high-quality from the tester to the DUT according to the design principle of antenna.

Second, wireless test provides the possibility of testing multiple DUTs simultaneously with one single test source so that test time is reduced and the utilization of tester's valuable resources is enhanced. The communications between the DUT and the tester are through antennas. Though the efficiency of on-chip antenna is low because of the limited area and lossy substrate, no constraints are put on the design of a high efficiency and high-power off-chip antenna. With such an off-chip antenna, the tester can transmit the signals to the DUTs in a quite large area, compared to the size of the chip.

Third, wireless embedded test is more reliable. Conventional tests often involve probing the wafer (chip) which can not only contaminate and damage the wafer (chip) but need additional RF bondpads, which result in more parasitics.

Finally, wireless test has the potential to reduce test system cost since it does not require a physical interconnection based on wires, connectors and RF probe cards.

2.3.2 Design Issues

The main limit of this wireless embedded test is that of the embedded test circuits themselves and it does not matter which off-wafer (chip) tester is used.

The embedded test circuit, however, is limited in size because of economic considerations. The test circuit is also limited by technology in its ability to operate at reduced power and voltage. The implementation of the proposed embedded test design must include some type of interface circuitry for input and output. It must also include the processing circuitry, which is capable of converting the input signal into the desired test stimulus without degrading the quality of converting the high frequency response into baseband signals.

This setup must be done with minimal power, voltage, and size so that it does not impact the circuit design. The power of the generated test stimulus must be kept low without compromising the signal quality, as this is the requirement of most RF/microwave tests. The size of the test circuits must be minimized to reduce the overhead costs associated with these test sites on wafers (chips).

Calibration of these on-chip test circuits is also an important issue. Calibration is a one-time effort which ensures testing circuits themselves work well before being applied to make normal measurements. Otherwise, when an error occurs, it is hard to say whether the DUT fails or not since it is possible to be a fault of testing circuits.

The introduction of on-chip test circuits should have as few effects on other circuits as possible. For example, without careful design and layout, the pararsitics accompanying the testing circuits will severely degrade the performance of the DUT during its normal operation.

All the design issues described above will be further discussed in the next several chapters when the detail designs of components in this proposed wireless embedded test are presented.

CHAPTER 3
RF RMS DETECTOR FOR EMBEDDED TEST

In an embedded test system, one goal is to accurately estimate the signal strengths. This is useful in (I) calibrating other test circuits, which ensures they work correctly, (II) measuring signals entering the circuit under test (CUT), which makes sure the magnitude of the input signal is within the desired specification of CUT and keep this value as a part of test results and (III) measuring signals out of the CUT. To a large extent, the accuracy of the test results is determined by the accuracy and calibration of the detector. Hence, for detectors employed in embedded test, besides the requirements on bandwidth, dynamic range and accuracy, calibratability and reliability should be considered as well.

Typically, two kinds of detectors are widely being used: peak detectors and rms detectors. Although an average value can be estimated in both cases, for the first one, the value is only accurate at the one chosen waveform type for which it is calibrated, usually sinusoid waves. And the latter can be applied to measure the power of different types of signals depending on the performance of the detector.

In this chapter, a new wide bandwidth RF RMS detector is presented as follows: first, the principle of operation is discussed; next, a detailed circuit design is described and a behavior model of the circuit is built with Verilog-A, followed by a comparison of simulation results between the proposed analog behavior model and transistor-level model (using parameters from the IBM 6HP process); then, the circuit error analysis and analog statistical analysis for the detector are reported; finally, a test setup and measurement results are shown to support the design.

3.1 Introduction

The RMS amplitude is a consistent, useful and standard way to measure and compare dynamic signals of all shapes and sizes. When incorporated into embedded RF test structures, compact RMS detectors can directly convert on-chip high frequency signals to baseband signals, which can then be measured by low bandwidth test systems. Thus, low-cost test implementations for RF systems can be developed.

RMS detectors of various designs can be found in many applications in the fields of communication and of measurement systems. RMS detectors based on Joule heating provide good accuracy and wide bandwidth. However, the rather complex packaging requirements do not lead to a low-cost test solution. Diode detectors based on the square-law are traditionally employed in communication systems as a form of power measurement because of their favorable high-frequency performance and low-cost. However, elaborate compensation techniques are required to make them meet the demands of most applications. Dynamic range and temperature stability also limit their application.

Another choice for RMS detector designs is based upon the translinear principle. Compact integrated versions of such circuits are described in references [See84, Was88, Mul97, Kum98 and Car01], which include both implementations using bipolar transistors [See84, Was88, Mul97 and Kum98] and MOS extensions [Car01]. A well-known example of the bipolar approach is presented by Mulder [Mul97], in which the authors merged both squarer-divider and low-pass filter blocks into one dynamic translinear loop, achieving a high-functional density. Since a full-wave rectifier is still required to precede the whole translinear loop, high-speed performance is severely degraded. A bipolar dual translinear-based RMS detector was described by Kumwachara and Surakampontorn

[Kum98]. The bandwidth was improved to 100 MHz without the requirement of the rectifier circuit. Carlosena [Car01] applied the MOS translinear principle to the design of a RMS detector. Although it has the advantages of implementation in a standard CMOS technology and very low supply voltage, the circuit can not match the corresponding bipolar circuits in performance.

For modern system applications, detectors with better performance are needed. It has been demonstrated [Mul97] that translinear circuits allow designs with high frequency and high-thermal stability, but this has not been realized in RMS detectors. In this chapter a monolithic integrated RF RMS detector is presented with wide bandwidth (up to Gigahertz) and that is stable with temperature [Yin04]. For a 40 dB input dynamic range, the relative errors of the output are within 2%. With the addition of a base-current-compensation circuit, the errors can be further reduced.

The chapter is organized as follows. First, the principle of operation is discussed. Next, detailed circuit design is described and behavior model of the circuit is built with Verilog-A, followed by a comparison of simulation results between the proposed analog behavior model and transistor-level model (using parameters from the IBM 6HP process). Then, the circuit error analysis and analog statistical analysis for the detector are reported. Finally, Test setup and measurement results are shown to support the design.

3.2 Design Principle for RF RMS Detector

The translinear principle is a practical way of implementing nonlinear analog circuits. Systematic analysis and useful applications of translinear circuits can be found [Mul97, See91]. Two key building blocks in an RMS detector are a squarer-divider and a low-pass filter. By use of the translinear principle, the two functions can be merged into

one translinear loop. In figure 3-1, if the nonideal properties of the transistors are negligible, the relationship between Iin and Iout can be represented by a nonlinear differential equation:

$$I_{in}^2 = I_o I_{out} + CV_T \dot{I}_{out} \tag{3-1}$$

where Io is the bias current. Solving for Iout,

$$I_{out} = \frac{I_{in}^2 / I_o}{1 + sCV_T / I_o} = \left\langle \frac{I_{in}^2}{I_o} \right\rangle \tag{3-2}$$

where the operator < > represents a time average. Thus, the output current becomes the mean-square of the input signal. The rms signal is obtained by performing a square-root operation on I_{out}. Since this is just a baseband operation, the operation can be put off-chip without affecting the performance.

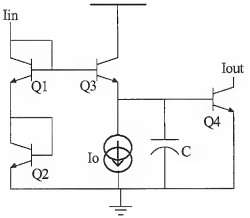


Figure 3-1. Basic translinear loop used in RMS detector.

In figure 3-1, I_{in}, flowing into the collector of Q1, has to be positive. To avoid using a rectifier and improve the high-frequency performance of the circuit, a DC bias current Io can be added to Iin, which eliminates the need for the rectifier ($|I_{in}| < Io$). In addition,

since it is more desirable to have voltage I/O signals than current I/O signals, a V/I input converter and an I/V output converter are integrated into the circuit. By avoiding any feedback loops in the circuit and separately optimizing the V/I conversion, a very wide-band operation is possible.

3.3 Design of RF RMS Detector Circuit

3.3.1. The Input Interface Circuit

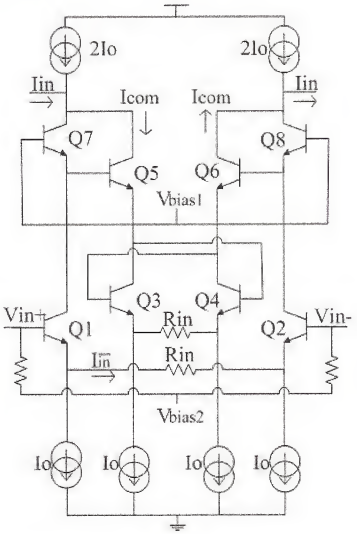


Figure 3-2. Input interface circuit and its matching performance.

To make sure the V/I converter does not affect the performance of the rest of the circuit, a wide-bandwidth converter has to be implemented. The circuit which the authors employed is shown in figure 3-2, the performance of which has been demonstrated by Caprio and El-Gamal [Cap73, Elg98]. $I_{\bar{m}}$ is given by

$$I_{\bar{m}} = \frac{V_{in}}{R_{in}} - \frac{V_{BE1} - V_{BE2}}{R_{in}} \tag{3-3}$$

The second term on the right side of the above equation represents the distortion of $I_{\bar{m}}$ due to the difference of V_{BE1} and V_{BE2}. The Caprio quad composed of Q3~Q6 provides feedback to reduce this effect, where

$$I_{com} = -\frac{V_{B5} - V_{B6}}{R_{in}} = \frac{V_{BE1} - V_{BE2}}{R_{in}} \tag{3-4}$$

By adding $I_{\bar{m}}$ and I_{com} together, the current I_{in} is obtained, which is a theoretically linear function of V_{in}.

The input referred noise is affected by the devices in the circuit. There exists a tradeoff between the linearity and the noise performance. The authors emphasize the former while keeping the noise low enough compared with the measurable input signal levels.

This input V/I converter can be operated in two modes: differential-mode and single-ended mode. For the differential-mode, the differential input voltage can be applied on the two sides and V_{in} becomes $V_{in} = V_{in+} - V_{in-}$. For the single-ended mode, an input voltage can be applied on one side and the other side is DC biased at a constant DC level.

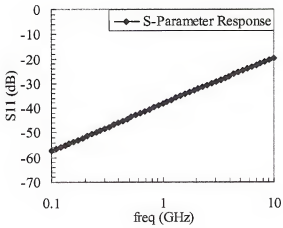


Figure 3-3. Simulation results of input S-parameter

For Gigahertz operations, input matching has to be emphasized. In practice, 50-ohm resistors shunted to ground on both sides will provide the best overall match (see Figure 3-2) for wide bandwidth applications. The simulated input s-parameters are shown in figure 3-3, which is good enough for the interested bandwidth. In addition, for improved testability of the circuit, a bypass capacitor should be added at Vbias1 for the differential-mode since it's not completely differential inside the circuit. In the single-ended mode, both Vbias1 and Vbias2 should be shunted with a bypass capacitor.

3.3.2. Squarer-divider and Low-pass Filter

Section 3.2 demonstrates the basic principles used to build a squarer-divider and a low-pass filter in one translinear loop. And a pair of differential currents was obtained from the input circuit discussed in Section 3.1, which is a linear function of the input voltage. Without using a rectifier, the sums of $Io \pm Iin$ ($|Iin| < Io$) are applied into two equal translinear loops as one is shown in figure 3-4. Therefore, according to the result of Section 3.2, the output currents of the loops can be obtained:

$$I_{out1,2} = \left\langle \frac{(I_o \pm I_{in})^2}{I_o} \right\rangle \tag{3-4}$$

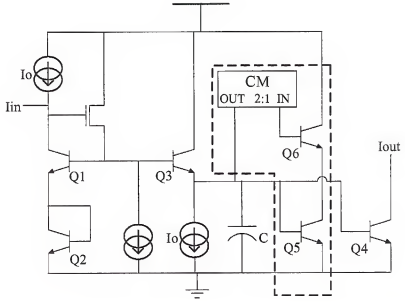


Figure 3-4. Translinear loop with base-current compensation shown in the dashed region (CM: current mirror)

The sum of the two output currents is:

$$I_{out1} + I_{out2} = \left\langle \frac{(I_o + I_{in})^2}{I_o} \right\rangle + \left\langle \frac{(I_o - I_{in})^2}{I_o} \right\rangle$$

$$= \frac{1}{I_o} \left\langle (I_o + I_{in})^2 + (I_o - I_{in})^2 \right\rangle$$

$$= \frac{2\langle I_{in}^2 \rangle}{I_o} + 2I_o \tag{3-5}$$

The average operation is linear and Io is a DC bias current. Therefore, if the DC current 2Io can be subtracted, the remaining part of the right side of (3-5) becomes the mean-square value of the input current multiplied by a scalar of 2/Io.

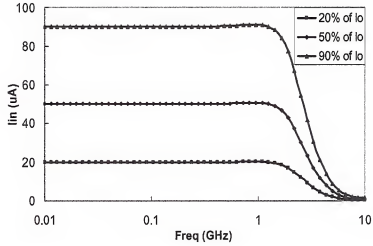


Figure 3-5. Frequency response at the input of the translinear loop

In figure 3-4, one translinear loop used is shown. The diode connection at the input of the loop is replaced by a NMOS helper transistor. This NMOS helper has two advantages over the bipolar helper transistor. First, it further reduces the base current error. Second, it brings better high-frequency performance than the bipolar helper if the size of the NMOS transistor and the bias current through it are carefully chosen. Only the left half of the translinear loop works in the high-frequency region. The simulated frequency response (using parameters from the IBM 6HP process) for the input is shown in figure 3-5.

3.3.3. The Output Interface Circuit

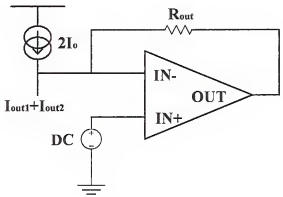


Figure 3-6. The output interface circuit

An output I/V converter is used to convert the current signal back to a voltage signal. Since at this step, the signal is low-frequency, the design of this converter becomes quite simple. It can be realized by a CMOS op-amp with a feedback resistor (see figure 3-6). The negative input terminal of the op-amp is connected to the output of two translinear loops and the other terminal is connected to a voltage bias, which is set to the collector voltages of the NPN bipolar transistors at the last stage of the translinear circuit. After offsetting the DC current 2Io at the output of the two translinear loops, the remaining current is converted into an output voltage. By suitably choosing the value of the resistor, Vout is the product of the mean-square value of the input voltage and a gain k.

$$V_{out} = \frac{2R_{out}\langle I_{in}^2 \rangle}{I_o} = k\langle V_{in}^2 \rangle \tag{3-6}$$

3.3.4. Error Analysis

The major sources of error in the circuit are in the translinear loop. Because of the finite current gain of bipolar transistors, the collector current of transistor Q3 will not be exactly (Io+Ic). This current error results from the base current of Q4 and Q3. Here, a new base-current compensation technique is introduced as shown inside the dashed part of figure 3-4. Without the base-current compensation circuit in the dashed block, the following can be derived:

$$\begin{aligned} I_{CQ3} &= \frac{\beta}{1+\beta}\left(I_0 + I_{cap} + I_{CQ4}/\beta\right) \\ &= \frac{\beta}{1+\beta}\left(I_0 + I_{cap}\right) + \underbrace{\frac{I_{CQ4}}{1+\beta}}_{error\ term} \end{aligned} \tag{3-7}$$

where β is the current gain of the bipolar transistors. With β around 100, which is a reasonable value for modern bipolar transistors, the first term on the right side of the above equation can be treated as the ideal value of Ic_{Q3} while the second term is the error term. Furthermore, this error term is a function of Ic_{Q4}. With the increase of Ic_{Q4}, it is easy to see from the equation of 3-7 that the error of Ic_{Q3} becomes worse. Considering the base-current-compensation circuit in the block with the assumption that all transistors are matched, a more accurate collector current of Q3 can be obtained from the following derivations:

$$I_{bQ6} = \frac{I_{CQ5}}{1+\beta} = \frac{I_{CQ4}}{1+\beta} \tag{3-8}$$

$$\begin{aligned} I_{CQ3} &= \frac{\beta}{1+\beta}\left(I_0 + I_{cap} + 2I_{CQ4}/\beta - 2I_{bQ6}\right) \\ &= \frac{\beta}{1+\beta}\left(I_0 + I_{cap}\right) + \frac{\beta}{1+\beta}\left(2I_{CQ4}/\beta - 2I_{CQ4}/(1+\beta)\right) \\ &= \frac{\beta}{1+\beta}\left(I_0 + I_{cap}\right) + \underbrace{\frac{2I_{CQ4}}{(1+\beta)^2}}_{error\ term} \end{aligned} \tag{3-9}$$

Comparing equation 3-9 with 3-7, the first terms on the right side of both equations are same while the error terms are different. It is obvious from equation 3-9 that the error of Ic_{Q3} can be reduced by a factor of $2/(1+\beta)$. Figure 3-7 shows the simulation results of RMS circuit with and without compensation subcircuit. From the figure, it can be seen that there is not much difference for the relative errors of two cases when the input signal is small. The relative errors become bigger for the rms circuit without the compensation subcircuit than that with the compensation circuit as the amplitude of the input signal increases. Hence, the compensation method is very effective

for reducing the base-current error resulting from Q4. Simulations demonstrate that the total relative errors of the output can be reduced to 1%. The complete RMS detector circuit is depicted in figure 3-8.

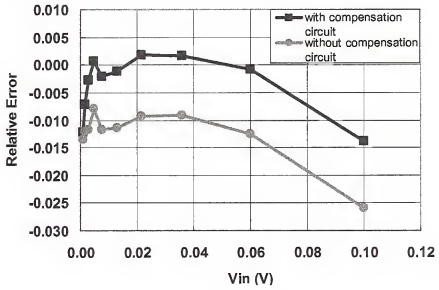


Figure 3-7. The simulation results of RMS circuit with and without compensation subcircuit for 1 GHz sinusoid input signal.

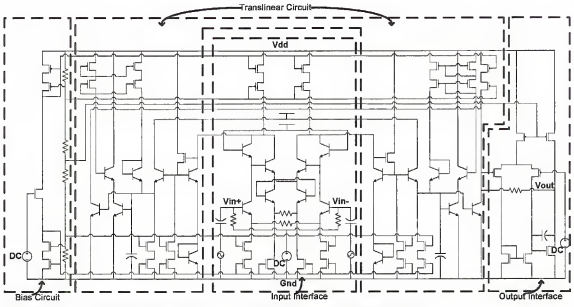
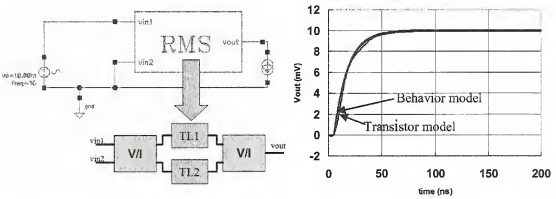


Figure 3-8. Complete circuit diagram of the proposed RMS detector.

3.4 Verifications of the RMS Circuit Design

3.4.1. Analog Behavior Model of the RMS Circuit



(a) (b)

Figure 3-9. Analog behavior model of the RMS circuit: (a) test fixture of analog behavior model; (b) comparison of simulation results between two models.

A behavior model is a way of defining the functionality of a design in terms of algorithms without describing its hardware implementation; behavioral models are based on sets of mathematical equations describing the behavior of a circuit element. A behavioral model is similar to a subcircuit object in that it constitutes a box which is connected to a circuit through electrical ports. Compared with transistor-level models, the difference is that the interior of a behavioral model box is implemented in terms of symbolic equations rather than a netlist, which greatly increases the simulation speed.

To verify the proposed RMS detector circuit design and to use the detector in "alternative test" methodologies [Var00], an analog behavior model is built based on the above analysis, which is shown in figure 3-9(a). With this model, the performance of the design can be accurately estimated without resorting to time-consuming transient analysis with transistor-level models. Simulation results of this proposed analog behavioral model are compared with simulations of the transistor-level model (using parameters from

IBM6HP process) in figure 3-9(b). The results of analog behavior model show small deviations from those of the transistor-level model only in the transient case, but have a good agreement in steady-state.

3.4.2. Monte Carlo Analysis of the RMS Circuit Design

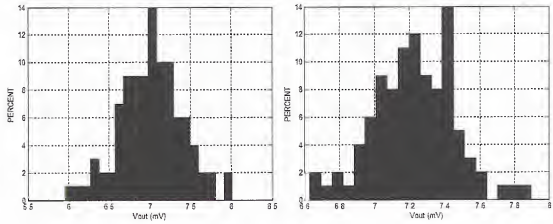
To account for process and mismatch variations, which play a more vital role on manufacturing yields as processes move to smaller geometries, corner simulations or Monte Carlo analysis can be applied on the proposed RMS circuit design.

Corners simulation tests for process, temperature, and mismatch variations. With this method, a designer determines the worst case corners, or conditions, under which the design will be expected to function. Next, each corner is simulated, and the output of each corner is examined to determine whether or not the design performs as required under each of the specified conditions.

The advantage of corner simulation is its relative simplicity. However, there are a number of issues with corner simulation. Perhaps the most troublesome of these is if the corners are not provided, then the designer may not know what the corners actually are, leading him to frequently make a best guess. Guessing worst case corners that will never occur in reality not only wastes design time, but also can result in a design that takes more area or consumes more power than needed, or even becomes impossible to design. Not guessing corners that will occur in reality may result in lower yield.

With Monte Carlo analysis, hundreds of simulations are typically run with a variety of variations introduced randomly, though; the guess work in determining the worst case corners is removed. Whereas corners analysis produces a binary outcome (either the corner passes or fails), Monte Carlo analysis produces samples of a continuous function that can be used to estimate yield. In addition, Monte Carlo deals with the distributions of

the process parameters among lots, wafers, and dies, and allows the designer to study the effect of parameter variations among devices on the same chip.



(a) (b)

Figure 3-10. Output distribution with process and mismatch variation: (a) with bias circuit; (b) with ideal bias (sample size 100, room temperature).

In the case of the proposed circuit design, since no worst case corners are available and the technology provided the statistical models, Monte Carlo analysis is preferred here. In the following analysis, the size of samples is 100 and a 1 GHz sinusoid input is assumed with 10 mV amplitude. Figure 3-10 (a) shows the RMS output values using Monte Carlo analysis with process and mismatch variation under the room temperature. It can be seen the variation of the output is around 15%. However, with all the bias circuits replaced by the ideal ones (Figure 3-10 (b)), it is found that the output variation decreases to 7%. This means the bias circuit is most vulnerable to process variation and mismatch. Therefore, to improve the yield of the proposed circuit, larger area bias current transistors need to be used. In addition, careful layout and employment of symmetric layout techniques can increase the yield further.

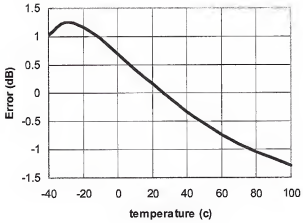


Figure 3-11. Variation of output .vs. temperature

The performance of the circuit under different temperatures is not examined with Monte Carlo analysis. Instead, output changes are obtained by transient simulations. From figure 3-11, it is found that the variation of the output is around ±1dB for temperature variation from -40 °C to 100 °C, which is acceptable for RF measurements. By examining the relation between the input voltage and output voltage in (3-6), it can be found this variation mainly results from the temperature variation of bias current Io. Hence, if the circuit supplying Io is improved to be independent of the temperature variation, it is expected that the variation of the output with temperature could be reduced further.

Since there exist process mismatch and variation for the design, from the above analysis, it can be seen the RMS detector needs to be calibrated first before it is applied for embedded test. Here one question arises: how to calibrate the detector which is integrated with the circuit under test?

The goal of the embedded test is to reduce the cost of on-chip RF test. Hence, the detector can not be calibrated via applying a very high frequency input signal to the chip with expensive RF probes. One simple approach is to use the wide band characteristics of

the detector. That is, the detector can be calibrated at low frequencies and then applied to measurements at higher frequency signals.

3.4.3. Simulation Results of the Proposed RMS Detector

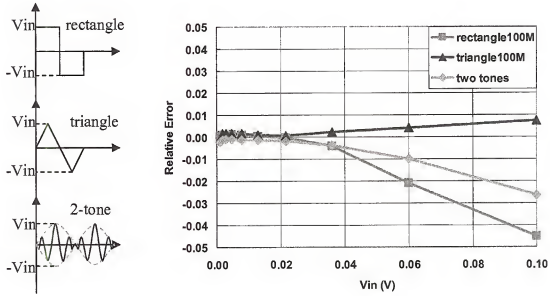


Figure 3-12. Simulated relative errors for different waveforms

To further verify the performance of the proposed RMS detector, simulations of transistor-level models (using parameters from IBM6HP process) are run with the SpectreS simulator.

Figure 3-12 shows the simulated relative errors for three waveforms other than sinusoid waveforms at 100 MHz. It can be seen that it's more inaccurate to detect the rms value of rectangular wave than that of triangular wave, especially at higher amplitude levels. The reason is that there is more peak energy in rectangular waves than in triangular waves. The two-tone simulation is performed with two sinusoid waveforms of same amplitude at 850 MHz and 900 MHz.

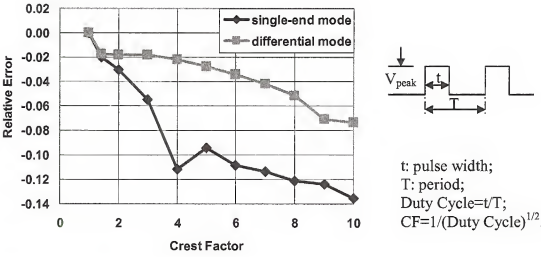


Figure 3-13. Relative error versus crest factor

As stated by Mulder [Mul97], the worst-case waveform for an rms measurement is a rectangular pulse train, where all energy is contained in the peaks. To perform simulations of the relative errors as a function of the crest factor, the duty cycle and the peak voltage of the applied input rectangular pulse train are varied to obtain different crest factors at some constant rms value and pulse width. The information required by simulations is displayed in table 3-1. In all simulations, a constant rms value of 10 mV is assumed and the pulse width of the peak is given as 500 ps. Figure 3-13 shows the results of relative errors with different crest factors.

The blue curve is obtained when the circuit is driven in a single-sided manner, e.g., the full input signal is applied to one input terminal and the other terminal is AC grounded. If driven with a balanced differential signal, the red curve is obtained, which obviously has smaller errors than with the single-end signal. Actually, regardless which kind of input waveform is, the highest accuracy is always obtained when a balanced drive

is used, which can be available by using a balun (balanced-to-unbalanced converter) or some other high frequency transformer external to the integrated circuit. This is partly because the resistor between two input transistors results in an unbalanced current distribution on the two sides, especially for higher operating frequency or bigger input resistor.

Table 3-1. Information for simulations with different crest factors

CF	V_{peak} (mV)	Duty Cycle (%)	Period (ns)
1	10	100	---
1.4	14	50.0	1
2	20	25.0	2
3	30	11.1	4.5
4	40	6.25	8
5	50	4.00	12.5
6	60	2.78	18
7	70	2.04	24.5
8	80	1.56	32
9	90	1.23	40.5
10	100	1.00	50

3.5 Test Setup & Measurement Results

The circuit was fabricated in the IBM 6HP BiCMOS process. The power supply is 3.4V and the DC bias current used in translinear loops is 100 uA. The capacitors of two low-pass filters are 48 pF each, which combine with the bias current to yield a cut-off frequency of 12.8 MHz. All components are integrated on chip, including input matching and bypass capacitors for RF testability of the chip. The total size of the chip is 0.912 mm^2 (1102 um×828 um) and the core circuit area is only about 0.07 mm^2 (290 um×250 um. And a photomicrograph of this design is shown in figure 3-14.

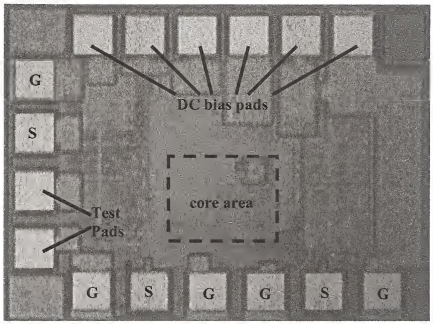


Figure 3-14. The microphotograph of the RMS circuit

There are totally 16 bondpads on the three sides of the chip. The bondpads of the top side (figure 3-14) are used for dc bias, each of which (except the ground pad) is shunted by an on-chip bypass capacitor of some suitable values. The goal of bypass capacitors here is to ensure the shunted terminals have good ac grounds since the parasitic inductance of the connection between the on-chip terminal and the external dc supply has to be considered in the very high frequency domain. The bondpads of the left side consist of output pads and pads for test. The input bondpads are at the bottom of the chip. (From left to right: G-S-G-G-S-G; G: ground, S: signal)

3.5.1. Test Setup and RF Calibration

It is quite easy to make DC measurements with semiconductor parameter analyzer. Besides setting the correct DC biases, the value of bias current Io is allowed to be observed by test pad and therefore it can be adjusted as required, which is important to the performance of the detector. A star grounding scheme is preferred to connect the grounds of all the instruments to a single point.

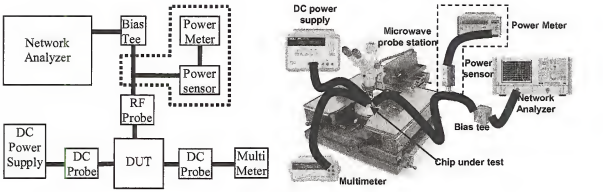


Figure 3-15. Basic RF test setup

Although it is simple to make DC measurements, to perform accurate RF measurements on the proposed detector is quite complicated. As seen in the left part of figure 3-15, a basic setup for RF measurements consists of a network analyzer, an ac or RF signal source (if not included in the network analyzer), an RF power meter and associated power sensor, a microwave probe station and probe heads, a bias Tee, DC supplies and multi-meters. A more visualable version of this test setup is shown in the right part of figure 3-15. The power meter and power sensor in the dashed block are only used for the power calibration of the network analyzer itself, not for the circuit measurements.

In the RF domain, the actual input signal power of the DUT (device under test) will be not equal to the one at the output of the signal source because of signal loss and reflection, both of which can be reasonably ignored in the lower frequency-domain. Therefore, the correct calibration and de-embedding processes have to be employed to obtain accurate experiment data. To a large extent, the correction procedure determines the final accuracy of the measurements.

The calibration procedure is to determine error-terms of the measurement system and sets a reference plane at the interface of the measurement system and DUT. With the help of network analyzer (Agilent PNA), the calibration process can be characterized into two steps: the source power calibration and the connection path calibration. Traditionally, people do not calibrate the power of the signal source; one reason is that all but s-parameters are energy ratios of incident and reflected power waves, and the other reason is that it is inconvenient to calibrate the source power with the traditional network analyzer, like HP8510, etc. Fortunately, the job becomes quite reasonable using the Agilent PNA with the details described in PNA manual [PNA02]. The calibration of the connection path as a whole can be done with the one-port calibration method introduced by Wijnen [Wij95]. At this stage, the reference plan is set to the end of the cable which connects to the probe head.

As for the measurements of s-parameters of this detector circuit, only the input port needs to be calibrated since the output always falls into the baseband. As a consequence, one-port calibration (open-short-load) is adequate for the measurements of the detector circuit. With the measured input s-parameters, the exact signal power entering the detector can be calculated assuming the correct calibrations, i.e. the reference plane is pushed to the tip of the probe head. The values of one-port s-parameter at 50 MHz and 1 GHz from -30dBm to 0dBm are shown in figure 3-16.

In the figure, it is reasonable to observe that the values of input return loss at 1 GHz are larger than those at 50 MHz since less of the signal is transmitted into the DUT at higher frequency for the same incident signal. All the one-port s-parameters are

approximately equal at the same frequency, which is found to be useful when measuring the frequency response.

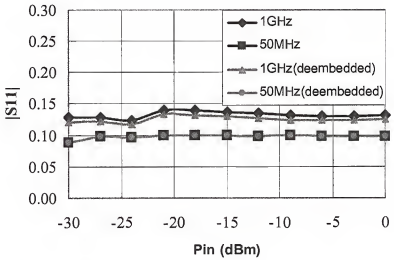


Figure 3-16. Measured one-port s-parameters at different frequencies

Further, the parasitics of the bondpads are included in the direct measurement of one-port s-parameter. If the circuit is applied for embedded test, then the input matching will become a little bit different since the input of the detector is connected to other circuit without the bondpads. To get rid of the effect of the bondpads, the s-parameters of a test structure of the bondpads is measured. The whole procedure is usually called de-embedding. Then, according to the theory of one-port network parameters, the de-embedded S_{11} parameter of the circuit can be extracted. The formulas used in this de-embedding procedure are listed below:

S-parameter → Y-parameter:

$$Y_{11} = \frac{1}{Z_0}\frac{1-S_{11}}{1+S_{11}}, \quad Y_{11bondpad} = \frac{1}{Z_0}\frac{1-S_{11bondpad}}{1+S_{11bondpad}} \tag{3-10}$$

Operation in Y-parameter domain:

$$Y_{11de-embedded} = Y_{11} - Y_{11bondpad} \tag{3-11}$$

Y-parameter → S-parameter:

$$S_{11\,de-embedded} = \frac{1 - Z_0 Y_{11\,de-embedded}}{1 + Z_0 Y_{11\,de-embedded}} \tag{3-12}$$

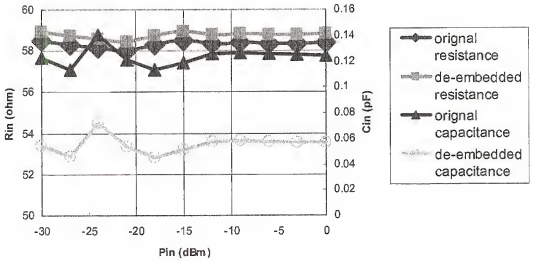


Figure 3-17. The de-embedded input impedance

The resulting one-port s-parameters at different frequencies are shown in red curves in figure 3-16 to compare with the un-deembedded ones. It is reasonable to note that the parasitics of the bondpads effect s-parameters more at 1 GHz than at 50 MHz. In the latter case (50 MHz), both the de-embedded curve and the un-deembedded curve are almost overlapped together. With some calculations, the input impedance can be obtained from the measured one-port s-parameters as shown in figure 3-17.

3.5.2. Measurement Results

Once all the errors are calibrated, accurate measurements are taken. The measured relative errors of the RMS detector output for DC signals, 50 MHz and 1 GHz sinusoid signals as a function of the input amplitude are shown in figure 3-18. The lower measurement level is limited by the accuracy of the measurement instrument, which is -

30 dBm provided by the ac signal source inside the network analyzer for the power sweep at a given frequency, and the upper measuring level is determined by the product of the bias current and the input resistor (Io×Rin), which can be seen in figure 3-19. The lower measurement level can be extended uses external attenuators.

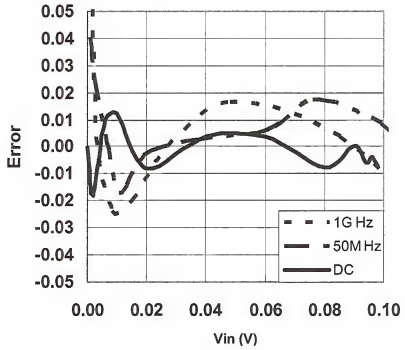


Figure 3-18. Measured linearity error .vs. different input signals

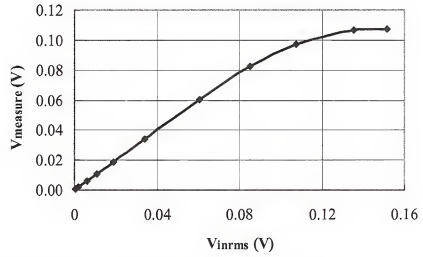


Figure 3-19. The upper measurement limit of the detector (measured at 1G Hz)

To investigate the bandwidth of the proposed detector, the calibrated frequency response of the circuit has to be measured. It was assumed that the input match parameters of the DUT are the same at each frequency independent of the power level of the input signal. The assumption can be justified from figure 3-16. With this assumption, the frequency response is obtained in figure 3-20. The measured –3 dB bandwidth is 1.3 GHz. The DC blocking capacitor causes a bit of rise of the curve.

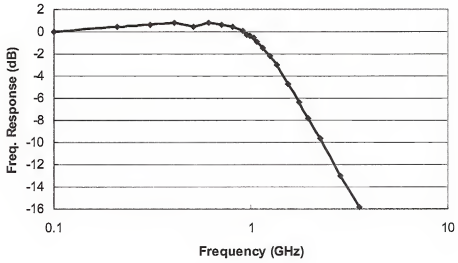


Figure 3-20. Frequency response of the proposed detector

CHAPTER 4
ON-CHIP COMPONENTS OF RF/MICROWAVE SIGNAL GENERATION

4.1 Introduction

From Chapter 2, it has been shown that one main challenge posed for today's RF/Microwave IC test is the need for on-chip generation of high-quality and high speed test signals using low-cost hardware. For this reason, this chapter demonstrates IC components which will be employed in a new scheme for on-chip RF/Microwave signal generation. Two components are presented in this chapter: an on-chip antenna and a frequency divider. The common features of these two components are simple and the capability of working at very high frequencies. The detail implementation of on-chip RF/Microwave signal generation will be left for the next chapter.

4.2 On-chip Antennas

As a critical component in the proposed wireless embedded test, the on-chip antenna is the subject of this section.

Traditionally, antennas are applied in such applications as long distance radio links and radars, in which large-sized and high-gain antennas are needed. While in the targeted application, the RF/Microwave signal source of the external tester can be very close to the wafer (chip) under test and the transmitted signal power can be enough strong, so that the size requirements of antennas are lowered. This gives an opportunity to mini-sized and low-gain antennas. As will be shown later, for an incident signal with a frequency above 20 GHz, an on-chip antenna with the length less than one tenth of the wavelength

still can be useful for short-range communication between the DUT and the external tester. From table 4-1, which gives the frequency versus wavelength in the following materials: air, dioxide, nitride and silicon, it can be seen that compared to the DUT, the size of such an antenna is small enough to be integrated.

Table 4-1. Signal frequency versus wavelength in millimeters for different materials

Frequency (GHz)	1.0	10	20	40	60	80	100
Wavelength (air)	300	30.0	15.0	7.49	5.00	3.75	3.00
Wavelength (dioxide)	150	15.0	7.50	3.75	2.50	1.87	1.50
Wavelength (nitride)	113	11.3	5.67	2.83	1.89	1.42	1.13
Wavelength (silicon)	86.9	8.69	4.35	2.17	1.45	1.09	0.87

Currently, the study of on-chip antennas is mainly researched in laboratories while it is gaining interest from industry. The on-chip antennas described in this work act as a receiver of external test signals. Next, the performance issues of on-chip antennas are discussed. Then the designs of various on-chip antennas are presented. These antennas are simulated with the aid of the EM simulation tool HFSS. The obtained simulation results of the antenna designs can be better explained how they will work in the real world before being manufactured. Finally, the test setup and the measurement results of the fabricated antenna test structures are demonstrated.

4.2.1 Performance Issues of Various Antennas

Conventionally, the performance of an antenna is characterized by its antenna impedance, radiation resistance, directivity, antenna gain and efficiency, all of which are summarized in table 4-2. Since all passive antennas are reciprocal, the same set of radiation properties can be applied to either transmitting or receiving capabilities of an antenna. Besides these properties of on-chip antennas, one key issue is large transmission

loss through silicon substrate. For most modern CMOS technologies, the resistivity of silicon substrate is in the range of 10 ohm-cm to 25 ohm-cm, which means the substrate is conductive at the usual working frequencies of on-chip microwave antennas.

Table 4-2. Parameters characterizing the performance of an antenna [Set97]

Antenna Impedance	The impedance measured at the input port of the antenna and is also called input impedance
Radiation Resistance	The ratio of radiated power to input current squared.
Directivity	The ratio of the maximum power density radiated by the antenna under consideration to the power density radiated by an isotropic antenna, both measured at the same range and excited by the same amount of input power
Antenna efficiency	The ratio of total radiated power to the input power supplied to the antenna and also called radiation efficiency
Antenna Gain	The ratio of EIPR to the input power, where EIPR is effective isotropic radiated power

To improve the performance of on-chip antennas, different types of antennas have been studied [Kim00, Oje04]. Some results obtained are summarized here:

The slot antenna consists of an aperture in a ground plan, where an electric field is excited across the slot. The straight slot antenna can be considered to be the complementary antenna to the dipole antenna, as shown in figure 4-1 (A) and (C), and many of its properties, such as input impedance, can be directly calculated from its equivalents. Typically, the slot antenna is an efficient radiator. But for on-chip implementation, it is of interest to keep the antenna ground-plane dimensions as small as possible, which inevitably compromises the performance. Another limitation is that the slot antenna is usually single-ended and thus not suited for connection to differential active circuits without the use of an on-chip balun.

Patch antennas, also called microstrip antennas, are metallic patches that sit on top of a dielectric substrate, as shown in figure 4-1 (B). Typically, they consist of a ground plane, a dielectric substrate and a patch. Usually, patch antennas are constructed from printed circuit materials so that they are thin with a low profile. Other advantages of these patch antennas are inexpensive, durable, conformable to various surfaces and versatile for resonant frequency, polarization, pattern and impedance. But a patch antenna manufactured on silicon will exhibit a small bandwidth and poor performance due to the high dielectric constant of the substrate. Conductive losses in the silicon will lead to poor efficiency, thus requiring the use of high resistivity silicon which is generally not compatible with standard SiGe bipolar and CMOS processes.

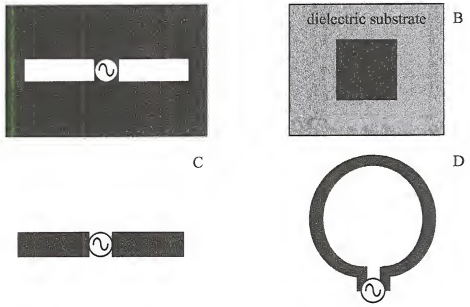


Figure 4-1. Four common types of antenna: (a) slot antenna; (b) patch antenna; (c) dipole antenna; (d) Loop Antenna

The dipole antenna is an alternative for on-chip antenna. It includes a variety of antennas, like folded dipole, linear dipole, meander dipole and zigzag dipole, most of

which are excited in the center. The dipole antenna has the same advantages for on-chip integration as the loop antenna. Usually the length of on-chip dipole antenna is less than half wavelength though ½-wave dipole is the most popular dipole. To further minimize the size of dipole antennas while minimizing the degradation on performance, the modified dipole antennas, such as zigzag and meander, were proposed by Nakano, Rashed and Ali [Nak84, Ras91 and Ali96]. Compared with the same-length linear dipole antennas, these modified dipole antennas have the higher gain and higher resonant frequency.

Loop antennas are usually circular turns of wire that radiate bidirectionally – along the axis of the loop or normal to its axis, as shown in figure 4-1 (D). They are suitable for on-chip integration because of two reasons: 1) The space that a loop antenna needs is limited, which can be easily understood, that if an antenna of given length is wound circularly it will be reduced in length; 2) A loop antenna is inherently balanced fed, which makes the antenna suitable for integration with differential circuit topologies without the use of on-chip baluns. In general, loop antennas have very low radiation efficiency because the radiation resistance is much smaller than the loss resistance, but which can be improved by using more turns of the loop.

Based on the above discussions, the loop antenna and the dipole antenna are more suitable to be integrated on-chip than other types of antennas. Lots of on-wafer measurements have been done to compare the performance of different types of on-chip antennas by SiMICS research group at University of Florida. From their measurement results, it has been seen that the best optimized performance results come from on-chip

zigzag dipole antennas [Li03]. Hence, the next subsections will focus on the implementation of on-chip zigzag dipole antennas.

4.2.2 Design Issues on On-chip Zigzag Dipole Antenna

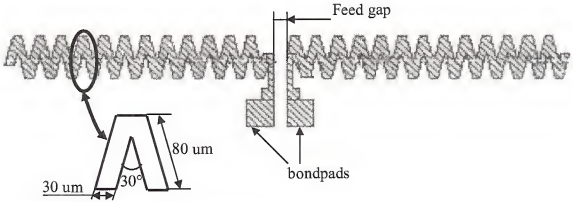


Figure 4-2. An on-chip zigzag dipole antenna

On-chip zigzag dipole antennas (shown in figure 4-2) with various length and metal levels are designed to compare their performance. The bend angle of these antennas, which is the angle between two neighboring arm elements of the antenna, is 30 degrees which is based on the optimized results from on-chip antenna measurements [Kim00]. The employed technology for design is SiGe 0.18 BiCMOS with the option of 7 metal levels. The lengths of designed antennas are 1mm and 2mm, respectively. For each length, a six-metal-level antenna and a top-metal-only antenna are implemented.

The resistivity of silicon substrate on which antennas are fabricated is in the range of 11 ohm-cm ~ 16 ohm-cm. There are seven metal layers in this technology, in which two metal layers are made of copper and the rest are made of aluminum. The top-metal-level antenna is made of the top layer of the metal, which is also the thickest metal (4.0 um) in this technology. By use of this thickest metal layer, it is expected that the loss

resistance through the antenna arms can be reduced so that the antenna efficiency can be increased. Based on the same target, multiple metal layers can be used in parallel in antenna design.

To make on-chip antennas more area-effective, the length of these antennas is usually designed to be less than half of the wavelength of incident signal, which means these on-chip antennas are not operating at resonance and hence the impedance of the antenna is not real when being matched to the following circuits.

One more point needs to be mentioned here is the feed gap, which is defined as the distance between two feed points as seen in figure 4-2. To improve both area efficiency and antenna efficiency, the gap should be as small as possible. However, if the gap becomes too small, two feed arms of the dipole antenna could couple with each other at very high frequency operation because of the parasitic capacitance between them. In our case, the antenna is operating around 24 GHz, and a reasonable feed gap can be chosen between 5 um ~ 30 um.

Apart from the above considerations, it is worth examining the effect of an on-chip antenna on the nearby circuits on the same chip. According to experiments and simulations [O04], this effect can be identified as noise coupling between the on-chip antenna and the integrated circuit elements through the common silicon substrate. Generally, the nature of this noise coupling is common-mode. Thereafter, to reduce this noise coupling, a symmetric IC layout relative to on-chip antenna is preferred and, meanwhile, the on-chip antenna itself is required to have a balanced structure and balanced feed.

4.2.3 Simulation Results of On-chip Zigzag Dipole Antenna

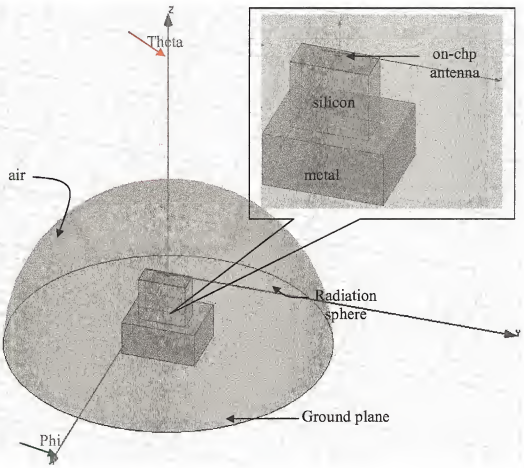


Figure 4-3. HFSS model of on-chip antenna

Figure 4-4. Layout of a 2-mm on-chip zigzag dipole antenna

Three different on-chip antennas are simulated with an EM (Electromagnetic) tool – HFSS (High Frequency Structure Simulator) as listed in table 4-3. The whole 3-D simulation model used in simulations is shown in figure 4-3. The radiation sphere is defined to allow waves to radiate infinitely into far space. At the bottom is an ideal ground plane. At the top right corner is the antenna chip model, which consists of four

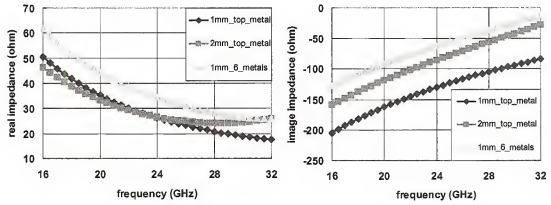
layers (from bottom to top): silicon, silicon-dioxide, silicon-nitrite and final passivation. The metals of which the antennas are made of are located inside the silicon-dioxide. The thickness of each level is given as physical dimensions which are obtained from MOSIS [IBM05]. Beneath the chip is a 2-mm metal layer, which touches the ground plane. More details about the building of antenna model can be found in related HFSS manuals [Ans05].

Table 4-3. Types of on-chip antenna manufactured

Type	Length (mm)	Metal levels used
1	1	Top Metal (MA)
2	2	Top Metal (MA)
3	1	6 Metal Levels (M1, M2, M3, M4, MT, MA)

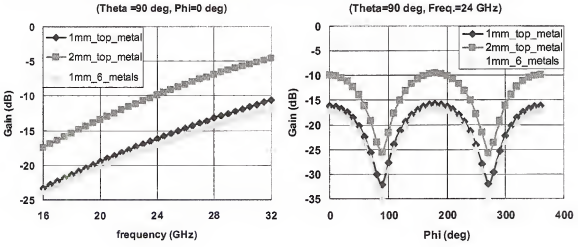
All HFSS simulations are performed with frequency sweep from 16 GHz to 32 GHz. The input impedances of different antenna designs are shown in figure 4-5 (a) and (b). From figure 4-5 (a), it can be observed that all the real parts of the antenna input impedance decrease with the increase of the signal frequency but the rate of decreasing becomes slower, for the case of type 2 antenna, the values even tend to increase from 28 GHz. The resistance of on-chip antenna is composed of radiation resistance and loss resistance. At the lower frequency end, the resistance of on-chip antenna is dominated by loss resistance, which explains that the 2 mm antenna made of the top metal has the lowest resistance and the resistance of type 3 is the highest among three antennas. This is also consistent with the results of figure 4-6, which shows the antenna gain varies with the frequency. In addition, the lower reactance of antennas made of the top metal due to lower metal-to-substrate parasitic capacitance contributes to their lower loss resistance as well. As the frequency increases, the radiation resistance becomes more important, which is proven by observing the real impedances of type 2 and type 3 become close and higher

than that of type 1 at the higher frequency end since the 2 mm antenna made of the top metal has the highest radiation resistance. In figure 4-5 (b), it can be observed that all the reactance parts of the antenna input impedance increase with the increasing of the simulated frequencies and are less than zero for the simulated frequencies, which means none of these on-chip antennas are half-wave antennas and they resonate at higher frequencies.



(a) (b)

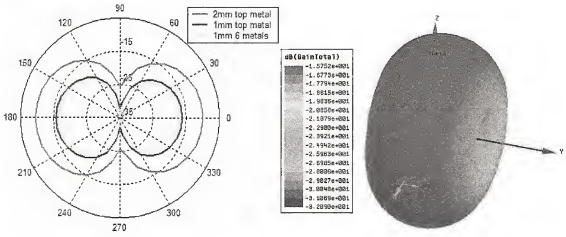
Figure 4-5. Simulation results of input impedances of different on-chip antennas



(a) (b)

Figure 4-6. Simulation results of antenna gain of different on-chip antennas

The simulated antenna gain for these on-chip antennas are displayed in figure 4-6 (a) and (b), where gain is defined as the ratio of antenna's radiation intensity in a given direction to the average power incident upon the antenna port. From figure 4-6 (a), it can be observed that the gain increases as frequency increases. The gain of 2-mm antenna is larger than that of 1-mm antennas at the same frequency. From figure 4-6 (b), it can be observed that the maximal gain occurs along the broadside directions. Furthermore, figure 4-7 (a) and (b) investigate the gain in the plane where the antenna locates and in the 3-D space, the shapes of which are similar to those obtained from usual half-wave dipole antennas.



(a) (b)

Figure 4-7. Antenna patterns: (a) antenna patterns in XY plane where the antenna locates; (b) 3-D antenna pattern.

It can be observed that the radiation patterns of all the treated antennas are bidirectional with maximums in the broadside direction and with back lobes of similar strength as the front lobes. The directivity of such antennas is generally less than 3 dB. The antenna gain is always lower than the directivity due to conductor and substrate losses in the antenna.

4.2.4 Measurement Results of On-chip Zigzag Dipole Antenna

Figure 4-8. Fabricated 2-mm on-chip zigzag dipole antenna

The test structures of on-chip antenna are made with an IBM process through MOSIS. Figure 4-8 shows the fabricated 2-mm on-chip zigzag dipole antenna. In practice, the test structures of both 2-mm and 1-mm antennas are fabricated. Two parameters are obtained in the test, which are antenna gain and input impedance. The test setup is shown in figure 4-9.

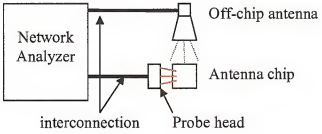


Figure 4-9. Test setup for on-chip antenna.

For input impedance measurements, on-wafer one-port calibration is performed first to a microwave probe through the network analyzer. Then, measured S-parameters are obtained and converted to the input impedances of the antennas, which are shown in figure 4-10.

The transmission gains of the on-chip zigzag dipole antennas are also measured using the test structure shown in figure 4-9. For the results plotted in figure 4-11, the separation between on-chip antenna and off-chip antenna is 6 cm.

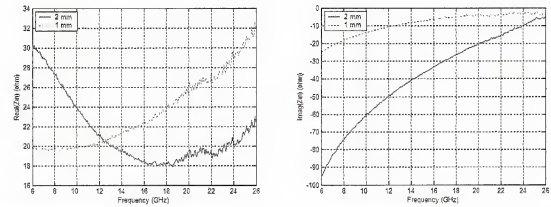


Figure 4-10. Measured input impedance of on-chip zigzag dipole antenna

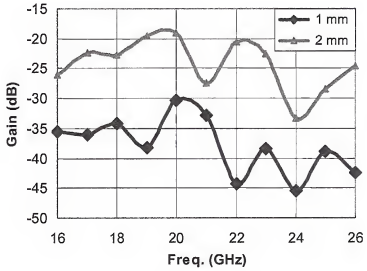


Figure 4-11. Measured antenna gain as a function of frequency

4.3 High-speed CMOS Frequency Divider

High-speed frequency dividers play a critical role in various wireless applications. For the implementations of frequency dividers, as shown in figure 4-12, there are

basically three configurations: 1) injection-locked dividers, 2) flip-flop-based dividers, 3) regenerative dividers.

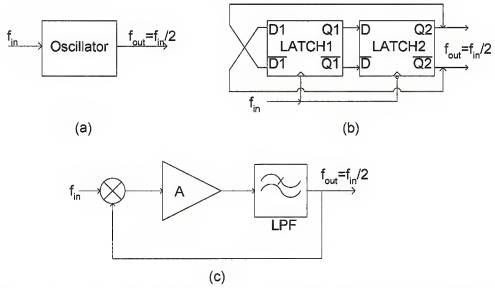


Figure 4-12. Frequency dividers: (a) injection-locked divider; (b) flip-flop-based divider; (c) regenerative divider.

Although all of these three frequency dividers have shown the capability of working at very high frequency in recently published papers [Tie04, Who02, Lee04], regenerative frequency dividers require many functional blocks to guarantee frequency division. As a result, they are not the best choice for embedded test circuits which emphasize on simplicity and area efficiency.

An injection-locked frequency divider is a free running oscillator which locks at the sub-harmonic of the injected input signal. The input signal can be injected through different nodes of an oscillator, and depending on the injection node, different injection-locked performances can be observed. Usually L-C oscillators are being studied as injection-locked frequency dividers since they are fast, simple, low power and low phase noise, though other kinds of oscillators can be injection-locked as well. Hence, most injection-locked frequency dividers in this chapter are based on L-C oscillators. One

more feature of injection-locked frequency divider is that the power level of input signal can be much less than that of the output signal. However, with the use of passive components, the area requirements need consideration for L-C oscillators at not very high frequencies.

Compared with regenerative dividers and injection-locked dividers, flip-flop-based dividers are static frequency diviers. They are comprised of two D-latches in cascade and in a negative feedback configuration as seen in figure 4-12(b). High-speed flip-flop-based frequency dividers are typically implemented using the current-mode-logic (CML) latches. Without using passive components, flip-flop-based frequency dividers achieve a wider bandwidth than other types of frequency dividers with smaller design areas. A major disadvantage associated with flip-flop-based frequency dividers is the high power dissipation especially at higher frequencies due to the proportional relationship between the power and operating frequency.

In this dissertation, frequency dividers are specifically used in wireless RF/Microwave test signal generation, which is required to generate a quite "clean" test signal from a "clean" while small amplitude input signal. Therefore, besides functioning as frequency-division, frequency dividers are also required not to degrade the qualities of the signal and have a good driving capability.

Based on the above concern and the discussion of different frequency dividers, when implementing the test signal generation, a frequency divider based on L-C oscillator can be used together with flip-flop-based frequency divider as well in the need of multi-stage frequency dividers.

To investigate the performance of frequency dividers, several designs of frequency dividers are manufactured with 0.18 um IBM technology, all of which are listed in table 4-4. The theoretical work of injection locking and pulling of oscillators is summarized in the next section. The design, simulation and measurement results of frequency dividers based on L-C oscillator are given in subsection 4.3.2. And in the subsection 4.3.3, the design, simulation and measurement results of flip-flop-based frequency dividers are discussed.

Table 4-4. Frequency dividers studied in this chapter

Index	Frequency Divider	Free Running Frequency	Comments
1	Injection-locked	5.6 GHz	NMOS-only L-C oscillator, single-ended injecting input
2	Injection-locked	12 GHz	NMOS-only L-C oscillator, Pseudo-differential-ended injecting input
3	Injection-locked	12 GHz	Fully differential stacked CMOS
4	Injection-locked	12 GHz	CMOS L-C oscillator with single-ended direct injecting input
5	Flip-flop	5 GHz	Fully differential CMOS without passive components

4.3.1 Injection Locking and Pulling of Oscillators

Many studies of injection locking have been published since the 70s in the last century [Adl73, Rat99, and Raz03]. But the date that the phenomenon of injection locking was observed can be traced back to as early as the 17th century, when Christian Huygens[1], confined to bed by illness, noticed that the pendulums of two clocks on the wall moved in unison if the clocks were hung close to each other [Raz03]. As a matter of fact, injection pulling and locking can occur in any oscillatory system, such as lasers, mechanical machines and electrical oscillators.

[1] Huygens is known for inventing the pendulum clock, discovering the nature of the rings around Saturn and numerous other accomplishments.

Here, only the injection locking of L-C oscillators are concerned. Sometimes, this phenomenon, also called injection pulling in communication system, is undesirable. For instance, as shown in figure 4-13, in an RF transmitter, when VCO and power amplifier (PA) are integrated on the same chip and the large output signal of the PA has the frequency close to that of a VCO, a portion of this signal can couple into the VCO through substrate and pull the VCO output, resulting in an unstable and noisy VCO output. Hence, the system and circuit approaches to reduce the interaction between VCO and incident signals are required, some of which can be found in the reference [Li04]. However, for the design of high speed frequency divider, injection locking can be proved to be a useful technique.

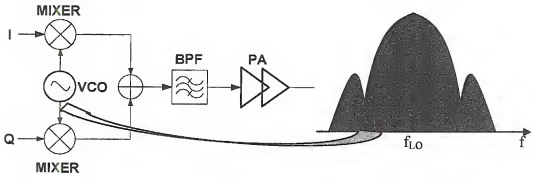


Figure 4-13. Injection pulling in an RF transmitter

A general model which is used to analyze the injection-locked oscillator is depicted in figure 4-14. Without the injection signal V_i, the model is just an autonomous system representing a free running oscillator. The nonlinear effects in the oscillator can be modeled as a function *F(e)* followed by a band-pass filter *H(ω)* with the center frequency ω_o at the free running frequency of the oscillator. Considering V_i injected into the model, with the well-known Nyquist criterion for oscillation (loop gain equal to 1 and phase shift equal to multiple of 2π), the Adler equation [Adl73], which is given by

$$\frac{d\theta}{dt} = \omega_o - \omega_i - \frac{\omega_o}{2Q} \cdot \frac{V_i}{V_o} \cdot \sin\theta \tag{4-1}$$

can be derived, where ω_i is the angular frequency of the incident signal, ω_o is the angular frequency of the output signal, Q is the quality factor of the L-C tank and θ is the phase shift between the output signal and the injection signal.

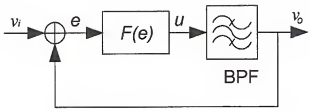


Figure 4-14. Injection-locked oscillator model

For the oscillator to be locked by the injection signal, the phase shift θ must remain constant with time. Therefore, from equation 4-1, the maximal locking range $\Delta\omega$ can be obtained as

$$\Delta\omega = 2(\omega_o - \omega_i) = \frac{\omega_o}{Q} \cdot \frac{V_i}{V_o} \cdot \sin\theta \le \frac{\omega_o}{Q} \cdot \frac{V_i}{V_o} \tag{4-2}$$

and with this expression of $\Delta\omega$, several design insights of injection-locked oscillator can be observed:

1) Operating frequency of the injection-locked frequency divider has little effect on the locking range since the quality factor of the oscillator will increase with the increasing of the operating frequency.

2) At the same operating frequency, the quality factor of the oscillator should be minimized to widen the locking range. The quality factor of an L-C oscillator can be approximately given by

$$\frac{1}{Q}=\frac{1}{Q_L}+\frac{1}{Q_C} \tag{4-3}$$

where Q, Q_L and Q_C are the quality factors of the oscillator, inductor and capacitor, respectively. For the oscillator working at below several gigahertzes, Q is dominated by Q_L so that using high-Q inductor directly leads a smaller locking range. For higher frequency regime, since Q_L is not much less than and even more than Q_C, more considerations need to be taken to adjust the quality factor of the oscillator.

3) The increasing of the injection signal can help the widening of the locking range. It can be easily understood that stronger the injection signal is, more efficiently it affect the oscillator. Intuitively, the performance of phase noise can be improved by the increasing of the injection signal as well, which will be discussed later.

4) The amplitude of the oscillator output signal should be limited to improve the locking range, which means that, without the injection signal, the oscillator should work at current-limited domain not voltage-limited domain. In this domain, the oscillator amplitude is solely determined by the tail current source and the tank equivalent resistance [Haj99].

5) The locking range is symmetric to the free running frequency of the oscillator. That is, the output center frequency of the injection-locked frequency divider is the free running frequency of the oscillator.

6) For the operation of a divide-by-n divider, ω_i in equations (4-1) and (4-2) should be replaced by ω_i/n and θ in equations (4-1) and (4-2) represents the relative phase shift between ω_i/n and ω_o.

The graphic solution based on the model in figure 4-14 can generate the same locking range as well. In this way, the input signal and output signal can be represented by phasors:

$$v_i = V_i e^{j(\omega_i t + \theta_i)} \tag{4-4}$$

$$v_o = V_o e^{j\omega_o t} \tag{4-5}$$

when locking happens, $\omega_i=\omega_o$ and θ_o is the phase shift between the input signal and the output signal. Further, if the phase shift between e and v_o is defined as φ and the phase shift contributed by bandpass filter is ψ, ψ should be equal to $-\varphi$ to satisfy Barkhausen's criteria.

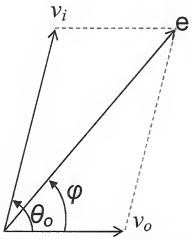


Figure 4-15 Phasor representation of injection-locked oscillator model

As shown in figure 4-15, φ can be represented by θ_o and the amplitudes of v_i and v_o, which is given by:

$$\varphi = \arctan(V_i \sin\theta_o / (V_i \cos\theta_o + V_o)) \tag{4-6}$$

The transfer function of bandpass filter can be represented by *H(ω)*.

$$H(\omega) = \frac{A}{1 + j2Q(\omega - \omega_o)/\omega_o} \tag{4-7}$$

Hence, the phase shift of *H(ω)*is:

$$\psi = -\arctan(2Q(\omega - \omega_o)/\omega_o) \tag{4-8}$$

From (4-6) and (4-8) and using the relationship between ψ and φ, it can be obtained:

$$\begin{aligned} &\frac{V_i \sin\theta_o}{V_i \cos\theta_o + V_o} = \frac{2Q(\omega - \omega_o)}{\omega_o} \\ &\Delta\omega = 2(\omega - \omega_o) = \frac{\omega_o}{Q} \frac{V_i \sin\theta_o}{V_i \cos\theta_o + V_o} \le \frac{\omega_o}{Q} \frac{V_i}{V_o} \end{aligned} \tag{4-9}$$

which is the same as the locking range derived from Adler's equation.

Furthermore, if the frequency of the injection signal falls out of, but not very far from the lock range, then the oscillator is said to be "pulled" [Raz03], as seen in the right part of figure 4-13.

Excellent phase noise performance is one of the major features to apply injection-locked oscillator as frequency divider. If there exists phase noise in an injection-locked frequency divider, then the input-output phase shift is no longer constant and can be written as

$$\theta = \theta_o + \theta_n \tag{4-10}$$

where θ_o is the constant input-output phase shift in the absence of noise and θ_n is the time-variant portion of θ, accounting for the additional noise. Substituting equation (4-10) into (4-1), it can be obtained that

$$\begin{aligned}\frac{d\theta_n}{dt} &= \omega_o - \omega_i - \frac{\omega_o}{2Q}\cdot\frac{V_i^{'}}{V_o}\cdot\sin(\theta_o+\theta_n)\\ &= \omega_o - \omega_i - \frac{\omega_o}{2Q}\cdot\frac{V_i^{'}}{V_o}\cdot\left[\sin\theta_o\cos\theta_n+\cos\theta_o\sin\theta_n\right]\\ &= \omega_o - \omega_i - \frac{\omega_o}{2Q}\cdot\frac{V_i^{'}}{V_o}\cdot\sin\theta_o - \theta_n\cdot\frac{\omega_o}{2Q}\cdot\frac{V_i}{V_o}\cdot\cos\theta_o\end{aligned} \tag{4-11}$$

where $V_i^{'}$ represents the sum of the injection signal V_i and injected noise V_n, and reasonable assumptions that both $\theta_o<<1$ and $V_n<<V_i$ are used. To express the above equation into the form of a transfer function of filter, with the help of equation (4-2) it becomes

$$\theta_n = \frac{\omega_o - \omega_i - \frac{\omega_o}{2Q}\cdot\frac{V_i^{'}}{V_o}\cdot\sin\theta_o}{j\omega + \frac{\omega_o}{2Q}\cdot\frac{V_i}{V_o}\cdot\cos\theta_o} = \frac{A}{1+j\frac{\omega}{\omega_C}}\cdot V_n \tag{4-12}$$

where

$$\begin{cases} A = \dfrac{\tan\theta_o}{V_i} \\ \omega_C = \dfrac{\omega_o}{2Q}\cdot\dfrac{V_i}{V_o}\cdot\cos\theta_o \end{cases} \tag{4-13}$$

Hence, the injected noise is shaped by a low-pass filter before it becomes the phase noise of the output signal, which is consistent with the results obtained by Rategh [Rat99]. The injection-locked frequency divider has the same noise transfer function as a first-order PLL. From equations (4-12) and (4-13), it is clear that the phase noise will decrease as the increasing of the injection signal, which intensifies the conclusion resulting from the analysis of the locking range.

Razavi [Raz03] explained from a time-domain perspective that the "synchronizing" effect of injection manifests itself as correction of the oscillator zero crossings in every period, thereby lowering the accumulation of jitter. He concluded that (1) the reduction of phase noise depends on the injection level, and (2) the reduction reaches a maximum for $\omega_i=\omega_o$. These two conclusions can be verified by our derivation as well. For example, when $\omega_i=\omega_o$, which means no phase shift between input and output, A in (4-13) approaches zero, which minimizes the gain of the phase noise transfer function and the phase noise is minimized.

In the following sections, the simulations and measurements of injection-locked frequency divider designs will be used to verify the above theoretical analysis.

4.3.2 An 11.2 GHz Injection-locked frequency divider

An 11.2 GHz injection-locked frequency divider was designed first, which uses a simple NMOS-only VCO structure, as illustrated in figure 4-16. The free running frequency of the VCO $\left(f_0 = 1/(2\pi\sqrt{LC})\right)$ is 5.6GHz. A 1.2 V V_{dd} and 4.6 mA bias current give a power consumption of 5.5 mW. The varactors in figure 4-16 are accumulation-mode nMOS capacitors. The quality factor of these varactors at 5 GHz is estimated to exceed 60. The quality factor of the LC tank is thus dominated by the inductors, as expected.

Before treating the circuit in figure 4-16 as a frequency divider, it is interesting to investigate the basic characteristics of it as a VCO. First, the relationship among V_{bias}, free-running frequency and output power is studied. Under the condition that the tuning voltage of the varactors is fixed and no injected signal is applied, figure 4-17 shows the measurement results of variations of free-running frequency and output power as a

function of the bias voltage. The bottom limit of V_{bias} is determined by Nyquist criterion for oscillation, the oscillation power at which is just above the noise floor. The maximum V_{bias} is limited by the maximum voltage which can be applied on the gate of MOS transistor M1, which is 1.8 V for 0.18um IBM technology. It can be observed that the free-running frequency of the VCO is almost independent of the bias voltage, especially at higher level of V_{bias}, which means the oscillation becomes more stable as V_{bias} increases. As for the output power, it increases as V_{bias} increases until V_{bias} reaches 1.0 V and then become saturated. This is reasonable since the output of VCO moves from current-limited regime to voltage-limited regime as V_{bias} increases [Haj99].

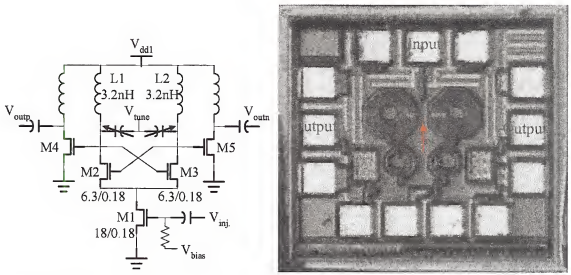


Figure 4-16. An 11.2 GHz injection-locked frequency divider based on L-C oscillator

The function of nMOS varactors is to tune the free running frequency of the oscillator by adjusting their control voltage. The voltage of nMOS varactor can be adjusted within a range of -0.5 V ~ 1.0 V. Figure 4-18 shows the measured tuning range and output power of the VCO. It can be observed that the VCO can achieve a 14% tuning range and contribute little to the variation of the output amplitude, which is less than 1

dBm within the whole tuning voltage range. Hence, with the help of the varactors, the bandwidth of the frequency divider can be extended.

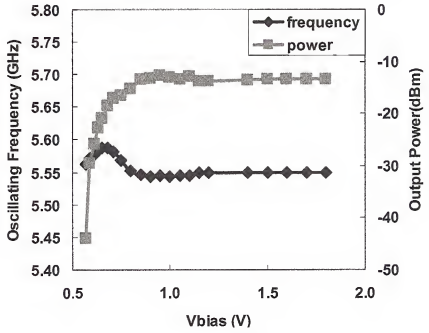


Figure 4-17. The measurement results of variations of free-running frequency and output power as a function of the bias voltage.

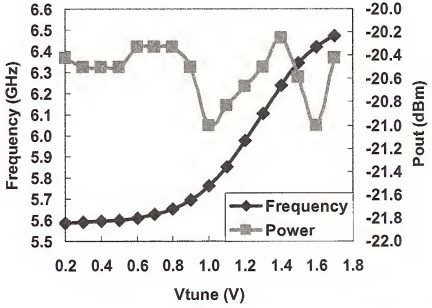
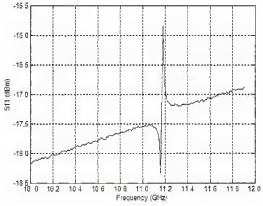
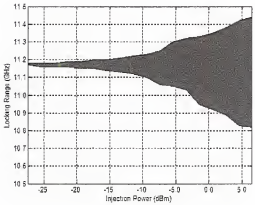


Figure 4-18. Oscillation frequency and output power as a function of varactor tuning voltage.

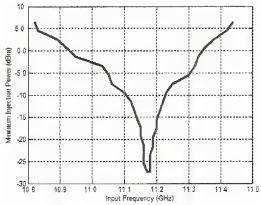
When the VCO in figure 4-16 is employed as a frequency divider, it becomes a non-autonomous system with an input serving as an injection point. Here, the injection point is chosen at the gate of transistor M_1 since (1) the required incident power can be reduced efficiently by injecting the signal to a high impedance node and (2) the common source connection of M2 and M3 oscillates at twice the frequency of the output signal even in the absence of the incident signal [Rat99].



(a)



(b)



(c)

Figure 4-19. (a) Measured S_{11} parameters; (b)Locking range as a function of incident signal power; (c) Relationship between minimum injection power and input frequency.

In addition, a wide-band input matching is formed by shunting a 50 ohm resistor with the gate of M1 as shown in figure 4-16. The stability of this input matching has been verified by measured S_{11} parameters at interesting input frequency band. The results are shown in figure 4-19 (a).

From measured S_{11} parameters, it can be observed that there is a glitch at 11.26 GHz, which is just at twice the oscillating frequency. This phenomenon further proves the selected input point is a natural injection point for divide-by-two frequency divider. Figure 4-19 (b) shows the locking range of this frequency divider as a function of injection power. As expected in theoretical analysis, the locking range increases as the injection power increases.

Figure 4-19 (c) is just another expressing form of figure 4-19 (b), which shows the relationship between minimum injection power and input frequency. Both of figure 4-19 (b) & (c) show the locking range is exactly symmetric with the free-running frequency of the VCO. And the injection power can be correctly estimated by use of

$$P_{inj.} = P_{measure} \cdot (1 - |S_{11}|^2) \tag{4-14}$$

where $P_{measure}$ is the signal power at the output of the signal source, and $P_{inj.}$ is the actual signal power injected into the VCO.

A comparison of the circuit in figure 4-16 working as a VCO and a divide-by-2 frequency divider is shown in figure 4-20, next to which is the test setup. To obtain a good phase noise performance, it is desirable to use battery to supply DC biases.

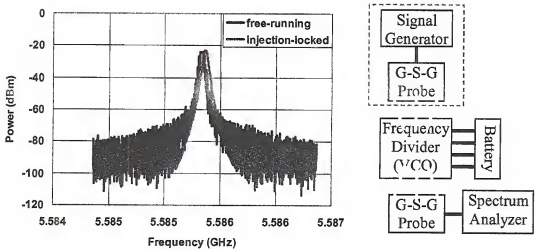


Figure 4-20. Measurement results of frequency sweep of oscillator as a VCO and a frequency divider.

4.3.3 A 24 GHz Pseudo-differential Injection-locked Frequency Dividers

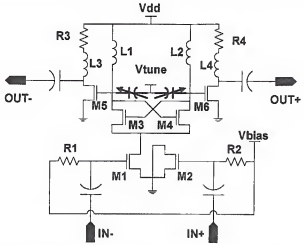
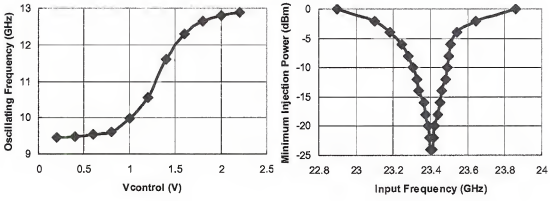


Figure 4-21. Pseudo differential injection-locked frequency divider

Considering connecting with other circuits, it is desirable to use differential-input frequency dividers. Here, a pseudo differential-input structure is used as displayed in figure 4-21. The measurement results of the fabricated circuit are shown in figure 4-22.



(a) (b)

Figure 4-22. Measurement results of pseudo-differential injection-locked frequency divider: (a) variation of free running frequency; (b) input sensitivity of frequency divider.

4.3.4 A 22.4 GHz Fully Differential Injection-locked Frequency Divider

Two topologies of differential injection-locked frequency dividers have been examined. Pseudo-differential divider can follow a differential circuit with the need of balun but the actual injected power is still the same as single-ended divider. Direct injection-locked frequency dividers can have a wide input locking range only for a large injection signal. So, is it possible to implement a real differential injection locked frequency divider with high input sensitivity?

From basic NMOS-only and PMOS-only injection-locked frequency dividers as shown in figure 4-23, it can be observed that, if the signals injected to both dividers are exactly the same except for a phase difference of 180 degrees, the outputs of both dividers can be connected together to form an output signal with larger swing. In this way, the topology in the right of figure 4-23 is proposed to form a stacked fully differential injection-locked frequency divider. The fabricated circuit is shown in figure 4-24.

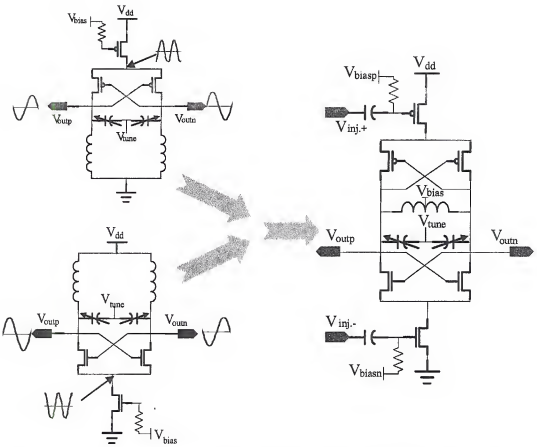


Figure 4-23. A stacked fully differential injection-locked frequency divider (new topology)

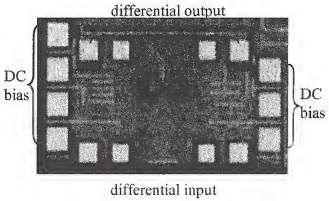
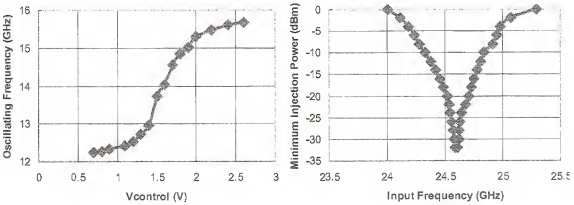


Figure 4-24. Photomicrograph of the proposed stacked fully differential injection-locked frequency divider

Furthermore, it can be proven that combining two basic frequency dividers of same type (NMOS-only or PMOS-only) does not work out because, in this case, the waveforms at the output nodes of both dividers can not have the same phase. This can be explained from the point of phase change as well. If the combined dividers are the same type, then the phase difference at outputs of two dividers is 90 degree for an input phase difference of 180 degree. Here the dividers are assumed to be divide-by-2. On the other hand, if two combined dividers are NMOS-only and PMOS-only, the phase difference at outputs of two dividers is 180 degree for an input phase difference of 180 degree since another 180 degree phase difference is added at the inputs of two dividers by the nature of using different types of injection transistor.



(a) (b)

Figure 4-25. Measurement Results of stacked fully differential injection frequency divider: (a) variation of free running frequency; (b) input sensitivity of frequency divider.

Figure 4-25 shows the measurement results of the proposed stacked fully differential injection-locked frequency divider. It can be seen that, compared to those of pseudo-differential divider, both input sensitivity and input locking range have been

improved since the actual power injected into the core has been increased about 3 dB for the same injection signal.

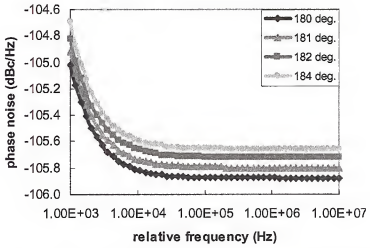


Figure 4-26. Simulated phase noise performance under the effect of the injected phase distortion

To investigate the effect of the injected phase distortion resulting from the different speed between input PMOS and NMOS transistors, simulations under various phase difference between two signals injected to the PMOS and NMOS tail transistors, respectively, as shown in figure 4-23, are run with spectre simulator. The resulted simulation phase noise performance is shown in figure 4-26. It can be seen that, for small phase distortions, which is the usual case for the phase distortion caused by different speed between input PMOS and NMOS transistors, the output still can be still locked to the input differential signal though the phase noise performance become a little worse.

4.3.5 A 24 GHz Direct Injection-locked Frequency Divider

Recently a new scheme to implement injection-locked frequency divider based on L-C oscillator is proposed [Tie04, Yam03], in which the incident signal is directly injected to the L-C tank through an extra transistor M4 instead of the tail transistor M1 as shown in figure 4-27. This injection scheme is believed to be more efficient at very high

frequencies because usually M1 has to be laid out with a large width to provide tail dc current and results in a large parasitic capacitance at the tail node, which includes C_{gd} and C_{db} of M1 as well as C_{sb} of M2 and M3. The effect of this parasitic capacitance becomes evident with the increase of oscillating frequency and lowers the effective injected power if the incident signal is injected through M1.

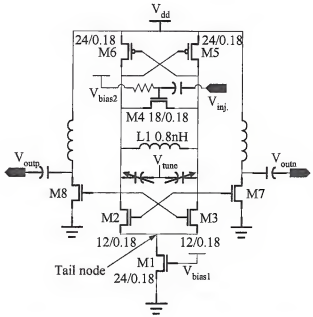


Figure 4-27. A 24 GHz directive injection-locked frequency divider

However, from simulations, it has been observed that the VCO can not be locked until the incident signal reaches a large power level, which can be explained examing the switching function of injection transistor M4.

The fabricated circuit is shown in figure 4-28. The measurement results are shown in figure 4-29. Compared with other types of L-C based injection-locked frequency dividers, direct injection-locked frequency divider requires a higher injection power to lock the frequency of input signal and the input locking range will not be enough wide until the injection signal reaches a high power level.

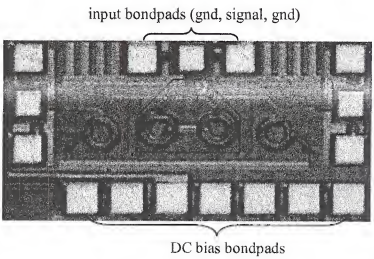
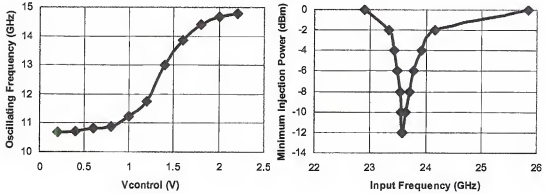


Figure 4-28. Fabricated direct injection frequency divider



(a) (b)

Figure 4-29. Measurement results of direct injection frequency divider: (a) variation of free running frequency; (b) input sensitivity of frequency divider.

4.3.6 A 10 GHz Flip-flop-based Frequency Divider

A flip-flop-based frequency divider is a wide-bandwidth frequency divider. Without using any on-chip inductors and capacitors, it consumes the smallest area among all kinds of frequency dividers. But it suffers from higher power dissipation with the

increase of operating frequency ($P \propto CV_{DD}^2 f$). Thereafter, it is advisable not to use the flip-flop-based frequency divider as the first-stage frequency divider.

For high speed operations, the structure shown in figure 4-30 is considered. As analyzed by Floyd [Flo01], this implementation can work in one of the two modes: standard digital mode and injection-locked mode. The digital mode of operation occurs for large input signals while injection-locked mode occurs for small input signal. Here, since the operation is in the range of small-level signals as far as the phase noise performance is concerned, the flip-flop-base frequency divider is used in injection-locked mode.

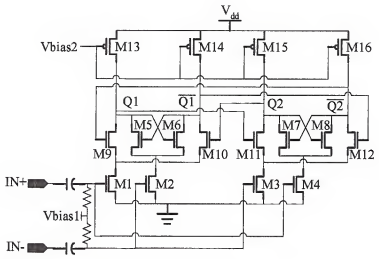


Figure 4-30. A 10 GHz flip-flop-based frequency divider

A test circuit with a 10 GHz flip-flop-based frequency divider has been made. Besides the transistors shown in figure 4-30, a pair of output buffers is added in the circuit design for the purpose of measurement. A photo micrograph of the fabricated circuit is shown in figure 4-31. There are five DC bondpads on the right side of the chip, which are corresponding to those terminals shown in figure 4-30 except for the power supply of the output buffer pair. Both of input and output are differential structures. The

total area of the circuit is 0.73 mm^2 (770 um*950 um), and the core area is only 448 um^2 (16 um* 28 um), which is composed of all the components in figure 4-30 except for the DC-decoupling capacitors and the input matching resistors.

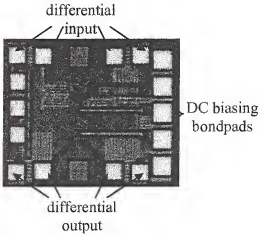


Figure 4-31. Photo micrograph of the fabricated flip-flop-based frequency divider

With the same dc biasing condition as in the simulation, the measurement results show, however, the self-oscillating frequency is only 3.6 GHz, and is lower than the simulated value, 5 GHz, which mainly results from the larger layout parasitic capacitance than simulation-based estimation.

Table 4-5. Input locking range of the cascade frequency divider .vs. injection power

Injection Power (dBm)	Input Locking Range (GHz)
-12	6.894 ~ 7.070
-8	6.804 ~ 7.138
-4	6.696 ~ 7.268
1	6.480 ~ 7.490
5	6.374 ~ 7.910

The measurement results of the input locking range under the different injection power are summarized in table 4-5. Compared with the input locking range of L-C

frequency divider discussed in the last section, the input locking range of the flip-flop-based frequency divider is larger at the same input injection power.

It has been known that increasing the power supply can increase the self-oscillating frequency of the flip-flop-based frequency divider. The measured self-oscillating frequency versus supply voltage is shown in figure 4-32. The maximum self-oscillating frequency can reach above 5 GHz for 2.8 V power supply.

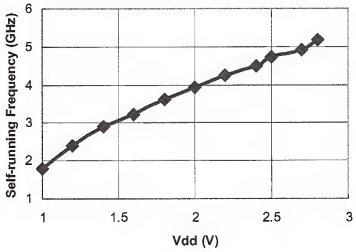


Figure 4-32. Measurement results of self-oscillating frequencies of the flip-flop-based frequency divider with different power supply

4.4 Investigation of Multi-tone Performance in Injection-locked Frequency Divider

The foregoing analysis, simulation and measurement of frequency dividers are based on the fact that there is only one-tone signal presented at the input of frequency divider, the frequency of which is nearby the twice self-oscillation frequency of the frequency divider. An interesting question is, "Is it possible for injection-locked frequency divider to handle two, three or more tone injected signals, assuming that all the

frequencies of these signals are around the twice self-oscillation frequency of the frequency divider?"

In this subsection, a theoretical analysis of injection-locked frequency divider with multi-tone injected signals is provided. Then, measured results of a divide-by-2 injection-locked frequency divider with multi-tone injected signals are presented.

4.4.1. Theoretical Analysis of Multi-tone Performance in Injection-locked Frequency Divider

A common model used to analyze the injection-locked frequency divider has been shown in figure 4-14. Without any changes, the same model can be employed to analyze the injection-locked frequency divider with multi-tone injection as well. To simplify the analysis, it can be assumed that the model represents a divide-by-2 injection-locked frequency divider. If a one-tone signal ($V_{i1} = A_{i1}\cos\omega_{i1}t$) is injected into the frequency divider and the output of the frequency divider is $V_o = A_o\cos\omega_o t$, this is a single-tone injection problem and can be easily shown [Rat99] that the output will be locked, i.e., $\omega_o = \omega_{i1}/2$ if the frequency of V_{i1} is within the locking range of the frequency divider.

Then, if a second-tone signal, which is within the locking range of the frequency divider as well, is added to the injection point, it is interesting to see if the output signals will be exactly two-tone signals with frequencies at the half of the input frequencies or other signals with different frequencies will appear at the output. Based on the model shown in figure 4-14, the following expressions can be obtained:

$$V_i = V_{i1} + V_{i2} = A_{i1}\cos\omega_{i1}t + A_{i2}\cos\omega_{i2}t \tag{4-15}$$

$$e = A_{i1}\cos\omega_{i1}t + A_{i2}\cos\omega_{i2}t + A_o\cos\omega_o t \tag{4-16}$$

$$u = F(e) = \sum_{n=0}^{\infty} a_n e^n \tag{4-17}$$

$$\frac{V_o}{u} = \frac{A}{1 + j2Q(\omega - \omega_r)/\omega_r} \tag{4-18}$$

Equation 4-17 represents the non-linearity function in the divider model, which is usually expressed as a power series, in which n must be at least equal to the order of the required locking [Jez74]. Equation 4-18 represents the bandpass function in the divider model, where A is the DC gain, Q and ω_r are the quality factor and free-running frequency of the frequency divider.

Since this is a divide-by-2 divider, from now on, *F(e)* is approximated as a third order nonlinear function (n=3), which allows the development of design insights,

$$u = F(e) = a_0 + a_1 e + a_2 e^2 + a_3 e^3 \tag{4-19}$$

where e is shown in equation 4-16, e^2 and e^3 can be expanded as follows:

$$\begin{aligned} e^2 &= (A_{i1}\cos\omega_{i1}t + A_{i2}\cos\omega_{i2}t + A_o\cos\omega_o t)^2 \\ &= A_{i1}{}^2\cos^2\omega_{i1}t + A_{i2}{}^2\cos^2\omega_{i2}t + A_o{}^2\cos^2\omega_o t + 2A_{i1}A_{i2}\cos\omega_{i1}t\cos\omega_{i2}t \\ &\quad + \underline{2A_{i1}A_o\cos\omega_{i1}t\cos\omega_o t} + \underline{2A_oA_{i2}\cos\omega_o t\cos\omega_{i2}t} \end{aligned} \tag{4-20}$$

$$\begin{aligned} e^3 &= (A_{i1}\cos\omega_{i1}t + A_{i2}\cos\omega_{i2}t + A_o\cos\omega_o t)^3 \\ &= A_{i1}{}^3\cos^3\omega_{i1}t + A_{i2}{}^3\cos^3\omega_{i2}t + \underline{A_o{}^3\cos^3\omega_o t} + 3A_{i1}{}^2A_{i2}\cos^2\omega_{i1}t\cos\omega_{i2}t \\ &\quad + \underline{3A_{i1}{}^2A_o\cos^2\omega_{i1}t\cos\omega_o t} + 3A_{i1}A_{i2}{}^2\cos\omega_{i1}t\cos^2\omega_{i2}t + 3A_{i1}A_o{}^2\cos\omega_{i1}t\cos^2\omega_o t \\ &\quad + \underline{3A_{i2}{}^2A_o\cos^2\omega_{i2}t\cos\omega_o t} + 3A_{i2}A_o{}^2\cos^2\omega_o t\cos\omega_{i2}t \\ &\quad + \underline{6A_{i1}A_{i2}A_o\cos\omega_{i1}t\cos\omega_{i2}t\cos\omega_o t} \end{aligned} \tag{4-21}$$

Then u will be passed through the bandpass filter with the center frequency at ω_r, which means only those terms in u close to the center frequency of this bandpass filter will present at the output while others are filtered out. It is easy to find the signals appearing

at the output from the first two terms on the right of equation 4-19. For e^2 and e^3, only the underlined terms in equations 4-20 and 4-21 include the signals to be presented at the output. These terms can be further expanded by replacing ω_{i1} with $2\omega_o$ and ω_{i2} with $2\omega_o + \Delta\omega_o$, where $\Delta\omega_o << \omega_o$ makes $2\omega_o + \Delta\omega_o$ within the input locking range of the divider.

$$2A_{i1}A_o \cos\omega_{i1}t \cos\omega_o t = A_{i1}A_o \cos 3\omega_o t + A_{i1}A_o \cos\omega_o t \tag{4-22}$$

$$2A_o A_{i2} \cos\omega_o t \cos\omega_{i2}t = A_o A_{i2} \cos(3\omega_o + \Delta\omega_o)t + A_o A_{i2} \cos(\omega_o + \Delta\omega_o)t \tag{4-23}$$

$$A_o{}^3 \cos^3 \omega_o t = \frac{A_o{}^3}{4}\cos 3\omega_o t + \frac{3A_o{}^3}{4}\cos\omega_o t \tag{4-24}$$

$$3A_{i1}{}^2 A_o \cos^2 \omega_{i1}t \cos\omega_o t = \frac{3A_{i1}{}^2 A_o}{4}(\cos 3\omega_o t + \cos 5\omega_o t) + \frac{3A_{i1}{}^2 A_o}{2}\cos\omega_o t \tag{4-25}$$

$$3A_{i2}{}^2 A_o \cos^2 \omega_{i2}t \cos\omega_o t$$

$$= \frac{3A_{i2}{}^2 A_o}{4}[\cos(3\omega_o + 2\Delta\omega_o)t + \cos(5\omega_o + 2\Delta\omega_o)t] + \frac{3A_{i2}{}^2 A_o}{2}\cos\omega_o t \tag{4-26}$$

$$6A_{i1}A_{i2}A_o \cos\omega_{i1}t \cos\omega_{i2}t \cos\omega_o t = \frac{3}{2}A_{i1}A_{i2}A_o[\cos(3\omega_o + \Delta\omega_o)t + \cos(5\omega_o + \Delta\omega_o)t]$$

$$+ \frac{3}{2}A_{i1}A_{i2}A_o[\cos(\omega_o + \Delta\omega_o)t + \cos(\omega_o - \Delta\omega_o)t] \tag{4-27}$$

Thus, if u is composed of u' and u'', where u' represents the part of u that is filtered out by the bandpass filter and u'' represents the part of u that reaches the output. From the above derivations, u'' can be obtained as below:

$$u'' = \left(a_1 A_o + a_2 A_{i1}A_o + \frac{3}{4}a_3 A_o{}^3 + \frac{3}{2}a_3 A_{i1}{}^2 A_o + \frac{3}{2}a_3 A_{i2}{}^2 A_o\right)\cos\omega_o t$$

$$+\left(a_2 A_{i2} A_o + \frac{3}{2} a_3 A_{i1} A_{i2} A_o\right)\cos(\omega_o + \Delta\omega_o)t + \frac{3}{2} a_3 A_{i1} A_{i2} A_o \cos(\omega_o - \Delta\omega_o)t \quad (4\text{-}28)$$

Therefore, three tones will present at the output: ω_o, $\omega_o + \Delta\omega_o$ and $\omega_o - \Delta\omega_o$. The divider will not function as a simple frequency divider any more with two input signals, even both of which are within the input locking range of the frequency divider. In fact, if the non-linearity function *F(e)* is represented by higher order power series, more frequency components will present at the output, which can be written as $\omega_o + n\Delta\omega_o$ and $n = 0, \pm1, \pm2, \pm3\cdots$, assuming all of them are within the pass band of the bandpass filter. $\Delta\omega_o$ is the frequency difference between two input signals and usually called the beat frequency. All the output components are spaced by this beat frequency.

As a special case, the components of the output can be examined when the injected input is an AM signal, i.e., $V_i = A_i(1 + m\cos\omega_i t)\cos\omega_c t$, where A_i is the amplitude of carrier, m is called AM depth or modulation index, ω_i is the modulation frequency and ω_c is the carrier frequency. This AM signal consists of three frequency components: ω_c, $\omega_c + \omega_i$ and $\omega_c - \omega_i$. If all these three frequency components are within the input locking range of the divider, it can be derived following the same procedure as the above analysis that the output signals will locate at $\omega_c / 2 \pm n\omega_i$ ($n = 0, \pm1, \pm2, \pm3\cdots$), which are within the pass band of the bandpass filter. Here, the modulation frequency ω_i becomes the beat frequency. If at the output, n is only allowed to take three values 0, 1 and -1, the output signal is still an AM signal but the carrier frequency becomes the half of the input carrier frequency.

4.4.2. Measurement Results of Multi-tone Performance in Injection-locked Frequency Divider

To verify the foregoing analysis, it is necessary to make measurements on the fabricated frequency divider by applying the multi-tone signal at its input. The experiments use the 12 GHz differential NMOS-only divider. The test setup is shown in figure 4-33.

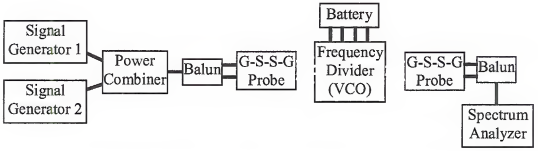


Figure 4-33. Measurement setup for multi-tone performance of injection-locked frequency divider

Here, two high frequency signal generators are used to supply a two-tone injection signal through a power combiner. The frequencies of two injected signals are 12 GHz and 12.002 GHz so that the resulted beat frequency is 2 MHz. The small beat frequency is chosen so that there will be more side bands presenting at the output of the divider, which makes it easier to compare with the above theoretical analysis. The amplitude of the second tone signal (12.002GHz) is set a little larger than the first tone signal (12GHz) as shown in figure 4-34. The reason will be explained later. The spectrum of this injected signal at the output of the power combiner is illustrated in figure 4-34. The free running frequency of the divider is adjusted to be about 6 GHz, which makes the injected signal locate at the middle of its locking range.

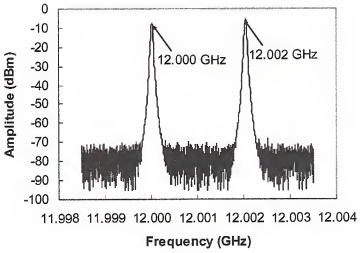


Figure 4-34. The injected two-tone signal to the frequency divider

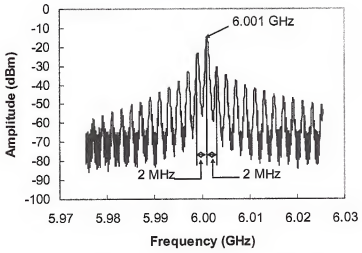


Figure 4-35. The resulted output spectrum of the frequency divider due to the injected two-tone signal

The output spectrum of the frequency divider due to this two-tone injection signal is shown in figure 4-35. It can be observed that the output signal is no longer a two-tone signal with frequencies at half of those of the input signal, which is consistent with the results of theoretic analysis. The theoretical analysis also suggests that the main band of the output should locate at the half frequency of one tone of the input signal and the side bands should be 2 MHz away from each other. From figure 4-35, it can be measured that

the main band locates at exactly 6.001 GHz, which is the half frequency of the second tone (12.002 GHz), and the beat frequency is 2 MHz as expected. Further, figure 4-35 proves that higher order sidebands are attenuated until they are completely filtered out because of the internal bandpass effect of the divider. In addition, it can be found by studying both figures 4-34 and 4-35 that the main band of the output locates at the half frequency of the stronger input tone, which can be intuitively understood since the stronger the input signal, more capable it is to be locked. This point is further verified with more measurements by adjusting the relative amplitude between two injection tones. If the two input tones are adjusted to have the exact same amplitude, the resulted output spectrum is shown in figure 4-36. In this case, the input is said to fail to lock the divider.

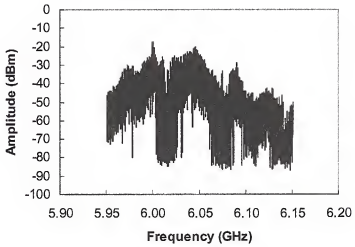


Figure 4-36. The output spectrum of the divider when the two-tone input has the same amplitude

The measurements of output spectrum of the divider due to injected AM signal are performed as well. The injected AM signal has the same form as that discussed in theoretical analysis. In measurement, the carrier frequency of AM signal is set to be at the center of the input locking range of the divider, AM depth is 25% and modulation

frequency (beat frequency) is 1 MHz. The spectrum of this AM signal is shown in figure 4-37.

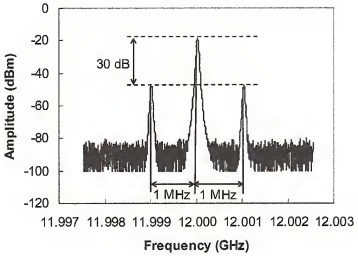


Figure 4-37. The spectrum of the injected AM signal to the divider

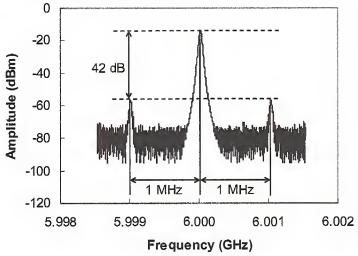


Figure 4-38. The output spectrum of the divider due to the injected AM signal in figure 4-37

The output spectrum is shown in figure 4-38. It can be observed that the output is still an AM signal. The carrier frequency of this output AM signal is 6.0 GHz, which is the half of that of the input AM frequency. As same as the input AM signal, two side bands of the output AM signal are 1 MHz away from the carrier respectively. However,

the relative amplitude from the carrier to two side bands is different between input and output. Again, this difference results from the bandpass effect of the divider itself.

4.4.3. Summary of Multi-tone Performance in Injection-locked Frequency Divider

In this subsection, the injection-locked frequency divider with multi-tone injection is studied. From the theoretical analysis, it is derived that the output of a two-tone injected divider behaves differently from that of single-tone injected divider. Besides the component at half frequency of the main tone of input signal, new frequency components will present every beat frequency away from both sides of divided main tone component, where beat frequency is the frequency difference between two input tones. A special case of three-tone injection signal is an AM signal, which is also discussed in theoretical analysis. The measurements of an L-C based injection-locked divider verify the validity of the analysis of frequency divider with multi-tone injection. In practice, measurements on flip-flop based frequency divider are performed as well and exhibit the similar results as those of L-C based frequency divider.

CHAPTER 5
AN INTEGRATED RF/MICROWAVE SOURCE AND ITS APPLICATION FOR EMBEDDED TEST

5.1 Introduction

A high-performance RF/Microwave source is a key component for commercial RF test equipment. Usually the source is designed to cover a wide range of frequencies and powers. In the initial stages of characterization, this flexibility is a necessary feature, which enables very rapid program changes. But once the part reaches the final stage of production, only a few worst-case frequencies or power levels are actually required to guarantee the performance of the device. The degree of purity and dynamic range of these few critical frequencies can directly effect the test time. Noise in the signal normally drives increased measurement averaging and increased test time. When the measurement requirement becomes very limited, such as the measurement of one tone next to a higher power tone, then a focused narrow band measurement circuit can often do a better job than a broad band one.

As for the proposed embedded test technique, based on the consideration of applications, complexity and area-efficiency, a narrow band on-chip RF/Microwave source is a plausible choice. As a matter of fact, most RF front-end components are operating in a specific frequency band, which are the target of the proposed embedded test. For example, a signal source working in the 2.4 – 2.5 GHz band would be enough if it is dedicated to testing Bluetooth or 802.11b devices only [Syl03]. Hence, it can be a waste of resource to apply a broad bandwidth signal source to measure a DUT with a

narrow bandwidth response. In addition, compared to a narrow bandwidth source, to design a wide-bandwidth source on chip usually requires a more complicated structure and more area, both of which are a disaster to realize in embedded test. Complicated structure for on-chip test circuitry will cause troubles on calibration. Without calibration, it is impossible to ensure the quality of RF embedded test. Big area consumption will increase the cost of embedded test, which makes this test methodology meaningless.

Based on the above considerations, this chapter describes the implementation of a very simple narrow-band microwave source, and then the application of this source is exploited for RF/Microwave embedded test. In the next section, current design approaches to implement on-chip signal generation are reviewed. Then, section 5.3 presents the design of this proposed on-chip microwave source [Yin05b]. The measurement results of the fabricated signal source are discussed in section 5.4. Finally, this signal source is applied to an embedded test scheme in which a 5.0 GHz LNA is tested.

5.2 Design Approaches for On-chip Signal Generation

It is a common way to use on-chip oscillators as simple on-chip signal generators, in which only dc voltages are needed to make the oscillator work. With the advent of smaller and faster CMOS technology, it has become possible to design very high frequency VCO in standard CMOS, for instance, the design of a 50 GHz CMOS VCO has been demonstrated by Wang [Wan01]. Therefore, the on-chip microwave oscillator-based approach demonstrates the capability of signal generation at such a high frequency. However, the off-chip inaccessibility makes the generated signal unstable, uncontrollable

and the resulting frequency drift is unpredictable. This is generally unacceptable for IC testing.

Another common way to generate an on-chip signal is to use phase-locked-loop (PLL), such as proposed by Yoneu [Yon05]. In this method, the generated signal is stabilized to some desired frequency by a feedback control performed by an on-chip PLL circuit, which uses an off-chip crystal oscillator as a reference signal. But the implementation of the PLL itself requires many functional blocks to guarantee its performance, which complicates the design. Furthermore, it will become more and more challenging to generate a signal with PLL-based approach with the increase of the operating frequency of the PLL over 10 GHz (which is possible at this time).

5.3 The Proposed 5 GHz Cascade RF/Microwave On-chip Source

5.3.1 Design Issues

The proposed RF/Microwave on-chip signal generation is very simple, and is only composed of an on-chip mini-antenna, frequency dividers and buffers, as shown in figure 5-1.

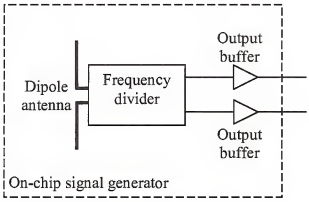


Figure 5-1. Block diagram of on-chip signal generator

With wireless communications between on-chip antennas and an off-chip antenna, the external signal can be transferred onto the chip where the receiver antenna is located. Since the external signal is provided by the specified signal source equipment, its characteristics can be precisely adjusted as required. Since the on-chip antenna is made of reliable passive components (metals), as discussed in chapter 4, the on-chip signal it generates can accurately track the transmitted signal with some power loss. Here, the important point is that the transmitted signal should be at very high frequency with enough power, which ensures the size of on-chip antenna (receiver antenna) to be as small as possible.

Although the gain of mini-on-chip antenna is very limited, with a reasonable power level of the incident wave, the signal regenerated by the antenna is still capable of locking the subsequent oscillator-based frequency divider if the half frequency is close enough to the free running frequency of the oscillator (see chapter 4). The stronger the injected signal is wider the locking bandwidth can be achieved.

Oscillators in this proposed signal source function as both frequency dividers and signal transformers, which means they change the frequency of the signal generated by the antenna into the DUT working frequency and amplify the signal without degrading the performance of the signal itself at the same time. Three important advantages can be appreciated from using frequency dividers in this on-chip signal generator. First, with the injection-locking nature of the frequency divider, the generated signal will be more stable and have less noise. Second, frequency dividers make it possible to employ a mini-antenna as an on-chip receiver since it is easier to implement an on-chip antenna with smaller size at higher frequency. In addition, the incident signal with much higher

frequency than that of CUT will have little CUT performance effect. Further, according to test needs, several frequency dividers can be cascaded together during the procedure of test signal generation.

The buffers at the last stage of signal generation in figure 5-1 serve as the interface between the source signal and the CUT. On the one hand, they separate the source from the other circuits so that the performance of the source will not be affected and simultaneously they ensure only the desired test signals are sent to the CUT and the bias information of signal source and the CUT are independent. On the other hand, they form impedance transformers so that the impedance looked into the buffer from other circuit approximates 50 ohm, which is critical for testing RF circuits.

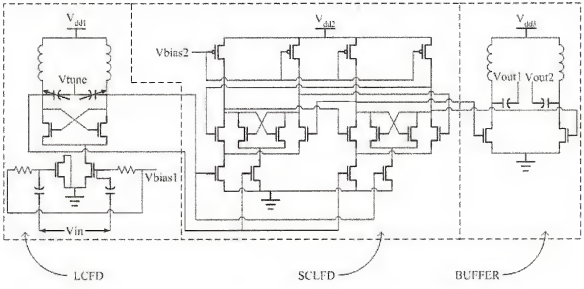


Figure 5-2. The schematic of two cascaded frequency dividers with output buffers (LCFD: LC-based VCO frequency divider; SCLFD: source-coupled logic frequency divider)

Figure 5-2 shows a two-stage frequency divider with output buffers. If the last stage of frequency dividers is an LC-VCO based divider, two output ports can be accessed by the CUT. With a flip-flop based divider (also known as source-coupled logic

divider) as the last stage, however, as many as four output ports can be accessed, though only two output ports are displayed in figure 5-2. Both of these dividers are analyzed in chapter 4. The output ports can be either connected directly to the CUT as the test signal source or connected to RF detectors, which monitor the performance of the on-chip signal source.

Although the biases among the last stage frequency divider, CUT and detector are separated by buffers, the biases among the cascaded frequency dividers can be reused. As shown in figure 5-2, with careful design, the dc bias Vdd1 of the output of LC VCO divider can be used as well to bias the input NMOS transistors of the next stage frequency divider. In this way, not only the intermediate buffer stages between the frequency dividers are saved, but the quality of signal is not degraded without the buffer. While the output buffer brings some degradation of the signal, the signal is still pure enough compared to meet the requirements for most RF test signals, which can be shown by simulation results in the next subsection.

5.3.2 Simulation Results

The simulation results of an on-chip RF signal source design are shown in figure 5-3, which includes an on-chip antenna working around 23 GHz, two cascaded divide-by-2 frequency dividers and output buffers. So the final output signal after the output buffer is around 5.5 GHz. The bandwidth of this signal generator mainly depends on the power of incident signal, bandwidth of antenna, and VCO tuning range.

Without considering the on-chip antenna, the schematic shown in figure 5-2 is simulated with Spectre-S. Input signals are provided with a pair of ideal differential signal sources instead. All the bias voltages are set as in the table 5-1.

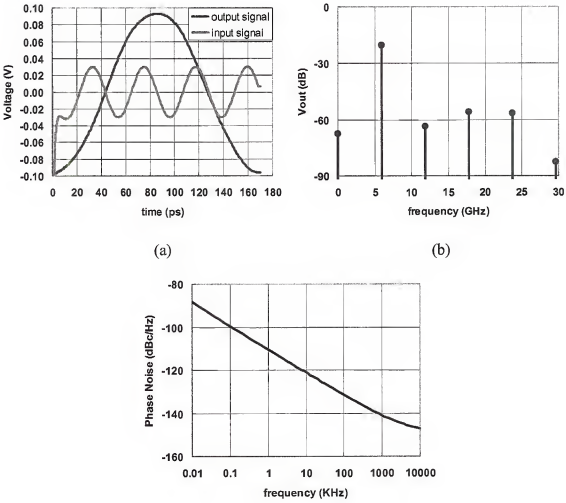


Figure 5-3. Simulation results of the schematic in figure 5-2; (a) input and output transient waveforms; (b) frequency harmonics of output signal; (c) phase noise performance of output signal.

Table 5-1. Bias setup & input signals of simulations for the schematic in figure 5-2

Parameter	Value	Parameter	Value
V_{in}	-20 dBm at 23.7 GHz	V_{tune}	0.85 V
V_{bias1}	0.65 V	V_{bias2}	0.0
V_{dd1}	1.2 V	V_{dd2}	1.8 V
V_{dd3}	1.2 V		

Figure 5-3 (a) shows the waveforms of one-period output signal and four-period input signals since the frequency of output is one-fourth of that of input. Five frequency harmonics of the output signal are displayed in figure 5-3 (b). The signal power at fundamental frequency is about 45 dBm higher than that at second harmonic. In figure 5-3 (c), it can be seen that the phase noise performance of the generated source is improved greatly compared to simple VCO-based signal generation methods.

5.3.3 Measurement Results

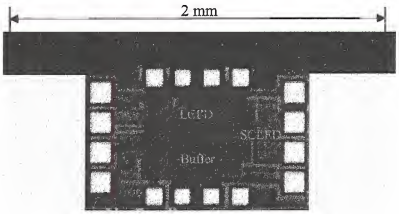


Figure 5-4. The photomicrograph of the circuit shown in figure 5-2 connected with an on-chip antenna.

The circuits shown in figure 5-2 connected with an on-chip antenna have been fabricated in IBM7WL process. The photomicrograph of the test structure is shown in figure 5-4, where the on-chip antenna is a 2-mm zigzag dipole antenna. To save space, it can be replaced by the one with smaller size. The structure of both top bondpads and bottom bondpads is ground-signal-signal-ground. The top bondpads are used to characterize the antenna when both of them are cut off from the rest of the chip. The bottom bondpads serve as the differential output terminals of the generated signal.

Without providing the incident signal from the off-chip antenna, the chip still can generate signals shown in figure 5-5 since the first stage divider itself is an oscillator in nature. However, in the figure there are more harmonics than expected. By inspecting in the frequency domain measurement, it is found that the second divider is unable to divide the signal at the output of the first stage. Rather, the self-oscillating signal generated by the second stage is shown up directly with its harmonics and the attenuated first stage signals. Figure 5-5 displays the first two harmonics generated by the first stage shown at the output of the second stage, the first three harmonics generated by the second stage, and a modulated signal generated by the fundamental signals of both stages.

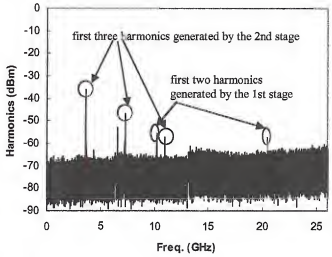


Figure 5-5. The output signal of the cascade frequency divider in frequency domain when the second stage is unable to divide the first stage output signal

With separate measurement of the test structure of LCFD shown in figure 5-4, it is found that the free running frequency of it can be tuned between 10.11~13.16 GHz, which is approximate to the simulated values. However, the free running frequency of the second stage dropped to 3.6 GHz while the simulations show 5.5 GHz with the normal supply voltage 1.8 V. The reduced frequency has been accounted for, due to larger

parasitic capacitance from the layout analysis. Thereafter, the second stage divider can not handle the signal at the output of the first stage since the frequency of the latter is not in the dividable range of the second stage.

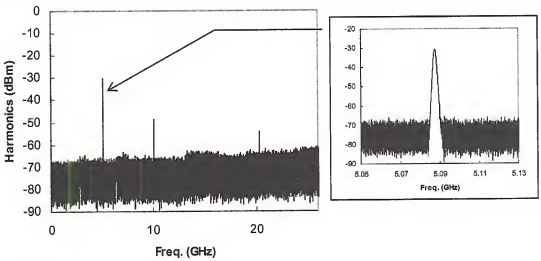


Figure 5-6. Harmonics of two-stage frequency dividers with the signal generated by the first stage divider

Fortunately, the free running frequency of the second stage can be increased by increasing its supply voltage (see chapter 4). Here, it can be shown from figure 5-6 that the output signal can be divided when the supply voltage of the second stage is adjusted to 2.7 V, which corresponds to a free running frequency of the second stage at 4.9 GHz. In this way, if the first-stage divider works at its lowest frequency when the varactor is adjusted to its maximum value, the output signal at the first stage can be exactly divided by the second stage as shown in figure 5-6.

In this figure, there are three harmonics observable from the spectral analyzer. Beside the strongest signal at 5.08 GHz, two other harmonics locating at 10.16 GHz and 20.32 GHz are leakage from the first stage, which are more than 20 dB below the

fundamental signal. The enlarged image of the fundamental signal is displayed in the right of figure 5-6 with a 100 MHz frequency range.

However, without some kind of external control, the signal at the output of the cascade frequency divider is not stable with time though it looks quite clean in the figure 5-6. Actually the signal will shift in a small frequency range from time to time. The source of this shift can be contributed by the free-running signal generated by the first stage, which demonstrates the necessity to give a control of the signal generation at the first stage. With the on-chip antenna connected to a suitable injection point at the first stage as shown in figure 5-4, an accurate off-chip signal can be injected to control the generation of on-chip signal.

Table 5-2. Input locking range of the cascade frequency divider .vs. injection power

Injection Power (dBm)	Input Locking Range (GHz)
-7	20.311 ~ 20.318
-2	20.308 ~ 20.320
3	20.301 ~ 20.325
8	20.291 ~ 20.333
13	20.269 ~ 20.348

With the same dc biasing as the measurement in figure 5-6, a signal generated by an external source is injected into the on-chip source through the off-chip and on-chip antenna pair. By adjusting the input signal power level, the input locking range of the on-chip source is obtained in table 5-2. The interconnection loss is considered in the calculation of the input power except the antenna loss. It can be inferred that the locking range can be further widened if the matching of the two stage dividers is improved.

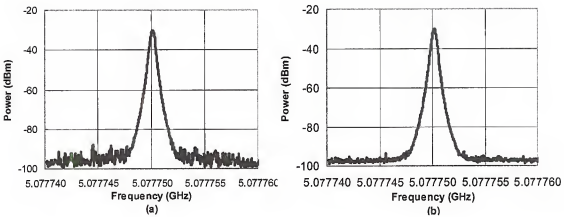
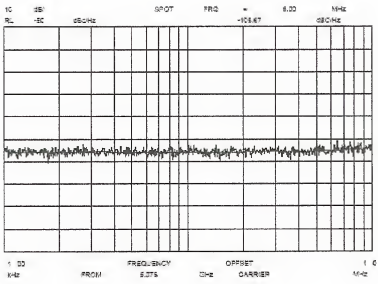
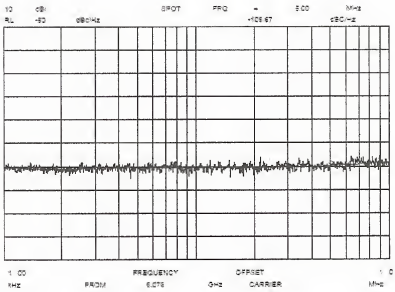


Figure 5-7. (a) Output signal of 5 GHz on-chip signal source; (b) 5 GHz output signal of external test signal generator.

To investigate the quality of the generated signal at the output of on-chip source, it is compared with a signal generated by an external signal generator. Figure 5-7 shows the measurement results of these two signals from the spectral analyzer with a 20 KHz band width. For the convenience of observation, the signal level from the external signal generator is adjested to be the same as that at the output of the on-chip source. In actual measurement, the output signal of the on-chip source is obtained by applying a 0-dBm signal from the external source to the off-chip antenna. The phase noise performance of both signals in figure 5-7 is illustrated in figure 5-8. It can be observed that both phase noise curves are almost flat in the whole measured bandwidth. For the signal generated by the on-chip source, the phase noise is around -106 dBc/Hz. And the phase noise of the reference signal, which is generated by the external signal generator, is -110 dBc/Hz. Hence the quality of the signal generated by on-chip source is comparable with that produced by the external source.



(a)



(b)

Figure 5-8. Measured phase noise using spectral analyzer: (a) signal generated by on-chip source; (b) signal generated by external source.

5.4 A 9 GHz single-stage RF/Microwave On-chip Source

Another implementation was done with a 9 GHz single-stage on-chip signal source. Without the second-stage SCL frequency divider, the received signal from on-chip antenna is divided only by an injection-locked L-C frequency divider. Figure 5-9 shows the measurement results from the spectral analyzer on the generated signal from the output of the on-chip source and the external signal generator. For the convenience of observation, the signal level from the external signal generator is taken to be the same as that at the output of the on-chip source. In actual measurement, the output signal of the on-chip source is obtained by applying a 0-dBm signal from the external source to the off-chip antenna.

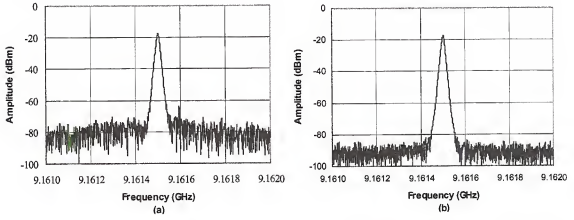


Figure 5-9. (a) Output signal of 9 GHz on-chip signal source; (b) 9 GHz output signal of external test signal generator.

5.5 Wireless Embedded Test for a 5 GHz Low Noise Amplifier

The previous parts of this dissertation discuss the designs, simulations and measurement results of each component of the proposed wireless RF/Microwave embedded test vehicle, including detectors, antenna and frequency dividers. In this section, a preliminary application of this wireless embedded test is explored.

5.5.1 Test Scheme for a 5 GHz Low Noise Amplifier

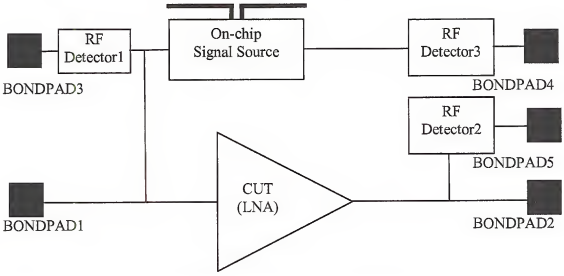


Figure 5-10. A new embedded test scheme for LNA measurement

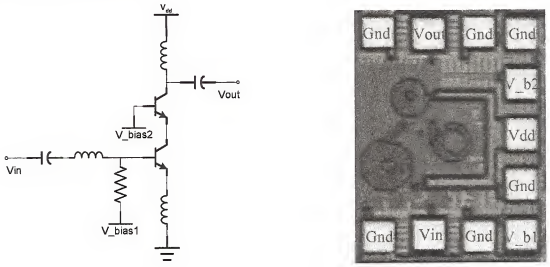
The low noise amplifier (LNA) is the most common component in RF front-end circuits. For communication systems, the LNA usually serves as the first stage in the receive path and it is supposed to be capable of processing signals with minimal noise and sufficient gain while probably driving 50 ohm.

With the proposed on-chip test signal generator and high frequency peak detectors [Zha04], it becomes plausible to characterize such a low noise amplifier within the chip. A proposed test scheme is displayed in figure 5-10. The wireless on-chip signal generator can supply two test signals simultaneously with 180 degree phase difference and the same amplitude within the operating frequency band of the LNA under test. Three on-chip detectors are employed in this test scheme, two of which are placed at two output ports of the generator respectively with one output port connected to the input of the LNA, and the third detector is placed at the output of the LNA. Bondpads 1 and 2 are RF bondpads, which are used only in normal operation of the LNA. In test mode, all test results can be directly obtained from three DC bondpads 3~5.

It will be shown later, with this test scheme, voltage gain, return loss, linearity and noise figure of a 5 GHz LNA can be investigated.

5.5.2 Low Noise Amplifier under Test

A low noise amplifier (LNA), which is used as the test object, is implemented using the same technology as that of on-chip test signal source and detectors. The LNA is made of bipolar transistors using the cascode structure, as seen in figure 5-11 (a). The input transistor is biased at 0.9 V and the power supply is 2.8 V. Both input and output are matched to 50 ohm.



(a) (b)

Figure 5-11. (a) The schematic of LNA under test. (b) The photomicrograph of LNA under test.

To investigate the performance of the proposed test scheme, a separate test structure of this LNA has been designed and manufactured, the schematic and micrograph of which is shown in figure 5-11. With conventional RF testing method, the performance of this LNA can be characterized.

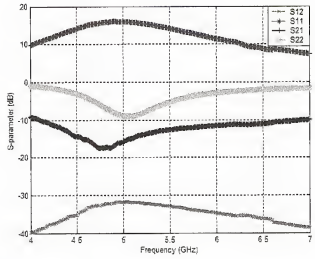


Figure 5-12. The measured S-parameters of a 5 GHz LNA

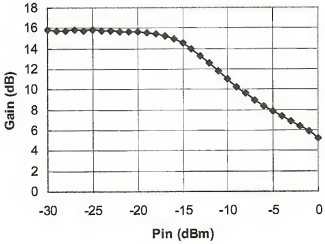


Figure 5-13. 1-dB compression point of 5 GHz LNA

Figure 5-12 shows the measured S-parameters of the LNA from 4.0 GHz to 7.0 GHz using a network analyzer. It can be observed that the maximum gain occurs around 5.0 GHz and the bandwidth for gain more than 10 dB is more than 2 GHz. The bandwidth for S_{11} less than -10 dB is also very wide and almost 3 GHz, covering the whole measure bandwidth. The S_{22} Measurement result is not as good as expected, which can be

improved using a more advanced matching network. In addition, the reverse isolation (S_{12}) is lower than -30 dB within the whole measured bandwidth.

The network analyzer can be used to investigate the linearity of an LNA as well. For this LNA, the 1-dB compression point is obtained using the measured s-parameters by sweeping the signal source inside the network analyzer. The power calibration of the signal source is made first from -30 dBm to 0 dBm at 5 GHz using an agilent PNA network analyzer. The measurement results are shown in figure 5-13, from which the 1-dB compression point of the LNA is located where the input power is -16 dBm.

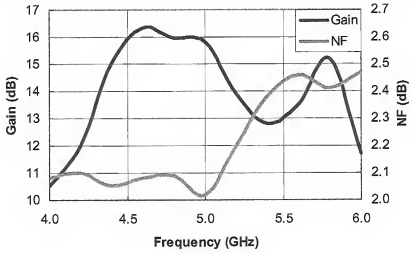


Figure 5-14. Noise figure and available power gain versus frequency.

Measurement results for noise figure is shown in figure 5-14 as well as the available power gain of the LNA. From this figure, the lowest noise figure can be found around 5 GHz and is approximately 2 dB.

Table 5-3. Summary of measured results for LNA at 5 GHz

Parameter	Result	Parameter	Result
S_{11}	-15.79 dB	P1dB (input)	-16 dBm
S_{21}	15.96 dB	NF	2.02 dB
S_{22}	-8.96 dB	Power Supply	2.8 V
S_{12}	-31.83 dB	Supply Current	3.1 mA

A summary of the measurement results characterizing this 5 GHz LNA is shown in table 5-3. Depending on the application, individual parameters of LNA can be further optimized. Here, the LNA is treated as an embedded test object, and the results obtained from the test are expected to be consistent with these direct measurements of LNA.

5.5.3 Theoretical Analysis of the Proposed Test Scheme

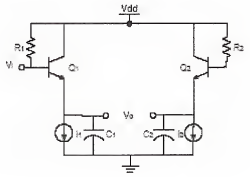


Figure 5-15. RF peak detector

Before the detailed theoretical analysis is discussed, several assumptions are provided:

- The RF peak detector is invasive, which means it is invisible to other components. This can be justified by the large input impedance seen into the peak detector as shown in figure 5-15.
- No catastrophic faults occur in the tested circuit. This guarantees the input and output impedances of the LNA are around 50 ohm in the region of operating frequencies and the imaginary part of the impedance is much less than the real part of the impedance.
- The LNA under test is unilateral, which means the gain from output to input is ignored. This can be justified by the measurement results of S12.

- The output impedance of the test source has been matched to 50 ohm over a wide bandwidth.

In the proposed test scheme, the detectors are used to detect the local voltages. Hence, all test results are voltage values. However, the results obtained from the conventional test are s-parameters. To compare the performance of the proposed test scheme with the conventional one, it is necessary to convert the s-parameters to voltage values or vice versa.

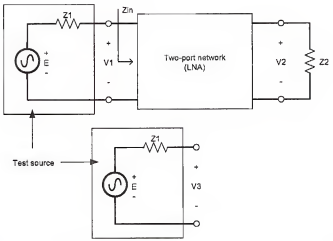


Figure 5-16. The equivalent network representation of the LNA test scheme

Figure 5-16 shows the equivalent network representation of the LNA test scheme. The test source is represented by a Thevenin's equivalent voltage source E and the associated source impedance Z_1. The LNA under test is represented by a two-port network. Z_2 is the load impedance at the output of the LNA. V_1, V_2 and V_3 can be measured by three detectors shown in figure 5-10, respectively.

From the properties of the two-port S-parameters and $Z_2 = Z_1$, it can be shown that E, S_{11}, S_{21} can be expressed as:

$$E = V_3 \tag{5-1}$$

$$S_{11} = \frac{2V_1}{E} - 1 \tag{5-2}$$

$$S_{21} = \frac{2V_2}{E} \tag{5-3}$$

Further, it's straightforward to build the relationship between S_{21} and the voltage gain V_2/V_1 of LNA by combining equations 5-2 and 5-3 and removing E. It follows that

$$\frac{S_{21}}{1+S_{11}} = \frac{V_2}{V_1} \tag{5-4}$$

This relationship between s-parameters and voltage gain can be applied to verify the linearity of LNA as well. The basic idea is to change the input power of LNA and observe the variation of LNA gain. In this way, the 1 dB compression point of this LNA can be located. The detail is shown in the next subsection.

Another important parameter in LNA design is noise figure. Normally, the noise figure of a LNA is defined as [Gon96]:

$$F = \frac{P_{N,o}}{P_{N,s} \cdot G_A} = \frac{P_{N,s} \cdot G_A + P_{N,LNA}}{P_{N,s} \cdot G_A} = 1 + \frac{P_{N,LNA}}{P_{N,s} \cdot G_A} \tag{5-5}$$

where $P_{N,o}$ and $P_{N,LNA}$ represent the total available noise power and the total available noise power due to the LNA itself at the output of LNA, $P_{N,s}$ represents the available source noise power and G_A is the available power gain of LNA.

One of the design goals of LNA is to minimize F so that $P_{N,LNA}$ is as small as possible. To obtain an approximated NF of the LNA under test, it can be assumed that the input and output impedance of the LNA are matched to 50 ohm so that $G_A \approx (V_2/V_1)^2$, and the extra noise generated by the LNA due to the imperfect realization is $\Delta P_{N,LNA}$. If the required noise figure and available gain are represented by F_{req} and $G_{A,req}$

respectively, then noise figure (F_{test}) generated by the proposed test scheme can be obtained.

$$F_{test} = 1 + \frac{P_{N,LNA} \pm \Delta P_{N,LNA}}{P_{N,s} \cdot (V_2 / V_1)^2}$$

$$= 1 + \frac{G_{A,req}}{(V_2 / V_1)^2}(F_{req} - 1) \pm \frac{\Delta P_{N,LNA}}{P_{N,s} \cdot (V_2 / V_1)^2}$$

$$\approx 1 + \frac{G_{A,req}}{(V_2 / V_1)^2}(F_{req} - 1) \qquad (5\text{-}6)$$

5.5.4 Measurement Results of the Proposed Test Scheme

With the foregoing analysis, it is shown that, by measuring the DC output voltages of three on-chip detectors, useful information about the LNA under test can be obtained.

The microphotograph of the whole on-chip test structure illustrated in figure 5-10 is shown in figure 5-17. The chip is composed of three main blocks: an on-chip test signal source, a LNA under test and on-chip detectors, which are ordered from left to right.

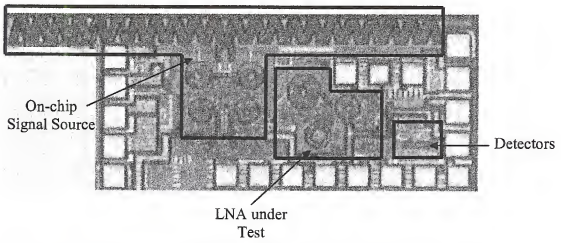


Figure 5-17. Microphotograph of the on-chip LNA test structure

When measurements are performed, off-chip components are obviated and all bondpads are DC bondpads. The required external test equipment includes a high frequency signal generator (Agilent E8254A), some DC power supplies and multimeters.

As discussed in section 5.3, because of the frequency mismatching between the first stage frequency divider and the second stage frequency divider in the on-chip signal generator, the measurable bandwidth of the generated signal is narrow, only about 10 MHz. However, a wider measurable bandwidth can be obtained with improved design.

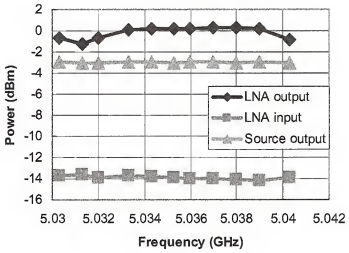


Figure 5-18. Measured output signals of three on-chip detectors

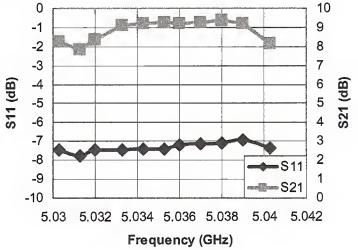


Figure 5-19. Derived s-parameters of the LNA from measured output voltage of detectors

The measured output voltages of three detectors represented in dBm are shown in figure 5-18. According to the analysis in section 5.5.3, the derived s parameters can be obtained in figure 5-19. Compared with the direct s-parameter measurements from the network analyzer, it can be seen that the derived S_{11} values are about 2 dB higher than measured S_{11} values, and the derived S_{21} values are about 2 dB lower than measured S_{21} results at the same input power level.

This difference could result from the following non-ideal effects. First, the input match of LNA will degrade in the presence of the shunted detector though it has been assumed that the detector is non-invasive. Second, the output impedance of the on-chip signal source is approximated as 50 ohm, but is not exactly 50 ohm, and will exhibit some parasitic reactance, which is different from the direct s-parameter measurement under the assumption that the source impedance is 50 ohm. Third, during the derivation of on-chip s-parameter measurement, the measurement of detector 3 (see figure 5-10) is treated as the open voltage of the signal source. This treatment is not very accurate especially at higher frequency due to various coupling effects and the lossy silicon substrate. In fact, it will be shown this is the biggest error source resulting in differences between the on-chip s-parameter measurements and direct s-parameter measurements using a network analyzer.

In addition, the voltages used in equations 5-1 to 5-4 are vector voltages while voltages measured from the output of on-chip detectors are scalar voltages. The resulting differences can be explained using the Thevenin equivalent circuit for an LNA input as shown in figure 5-20. Here, the on-chip test source is simplified as an ideal voltage V_s in series with a pure resistor R_s while the input impedance of the LNA is represented as Z_{in},

including both resistance and reactance. The measured input voltage is $(V_{in})_{measure} = V_s \cdot \left| \frac{Z_{in}}{R_s + Z_{in}} \right|$ while the vector voltage at input is $V_{in} = V_s \cdot \frac{Z_{in}}{R_s + Z_{in}}$. They are approximately equal only when $|Z_{in}| = \sqrt{R_{in}^2 + X_{in}^2} \approx R_{in}$. That is, using measured voltage values to estimate s-parameter is only valid when the impedance is dominated by its resistance.

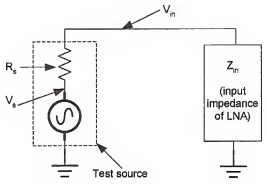


Figure 5-20. Thevenin equivalent circuit for LNA input

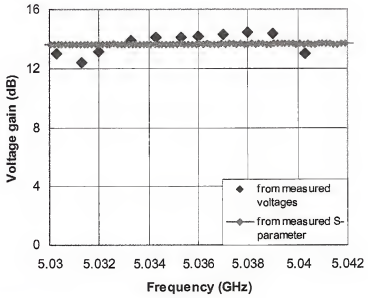


Figure 5-21. Voltage gain of LNA under test

The voltage gain of LNA can be obtained from the measurement results at the outputs of both detector 1 and detector 2 without the knowledge of signals presenting at the output of detector 3 and phase information of the input voltage and output voltage. To verify this voltage gain, direct s-parameter measurement results are transformed to voltage gain using equation 5-4. In this way, the inaccuracy introduced from the measurements at the output of detector 3 is ignored. The resulting voltage gain at the same input power (-14 dBm) from both on-chip measurements and direct S-parameter measurements is shown in figure 5-21.

It can be observed from figure 5-21 that the voltage gains obtained from the measured input/output voltages and from measured s-parameters are matched well. In the measurement range, all the errors are within +/- 1 dB. Compared with the s-parameter results shown in figure 5-19 using the measured output voltages of the third detector, this test is more accurate in characterizing the performance of LNA voltage gain. In the meantime, it indicates as well, that it is not a good assumption that the output voltage of the third detector represents the open voltage of the on-chip source. This suggests for the future work about how to extract the information of the output signal of on-chip source.

The above voltage gain curves are obtained by adjusting the frequency while keeping the same input signal power. If the voltage gain curve can be obtained by adjusting the input signal power while keeping the input frequency unchanged, the linearity of LNA can be investigated. From the analysis of the on-chip signal source, the power level of source's output signal can be varied in a certain range by adjusting the bias voltage of divider's tail transistor or adjusting the supply voltage of on-chip signal source's output buffers. If the input power of the LNA's 1-dB compression point is

within the variation range of the on-chip signal source's output signal power, then the linearity of LNA under test can be evaluated.

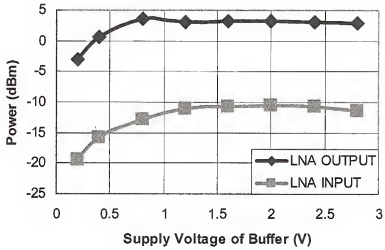


Figure 5-22. The adjustable power range of LNA's input and output

Figure 5-22 shows the adjustable power range of LNA's input signal and output signal by changing the supply voltage of on-chip signal source's output buffers. In the figure, the input power of LNA can be adjusted from -20 dBm to -11 dBm. It is already known that the 1 dB compression point of this LNA is at -16 dBm from on-wafer s-parameter measurement. Therefore, it is postulated that 1 dB compression point can be found within the measurement range of on-chip detectors' output voltage.

Illustrated in figure 5-23 is the power gain obtained by subtracting LNA input power from LNA output power in figure 5-22. The gain in linear region is a little higher than that obtained from direct s-parameter measurements. But the input 1 dB compression point is still nearby -16 dBm. Although no exact measured point is located

at P1dB point, it can be determined from the curve made of measurements, that the input 1 dB compression point is about -15 dBm.

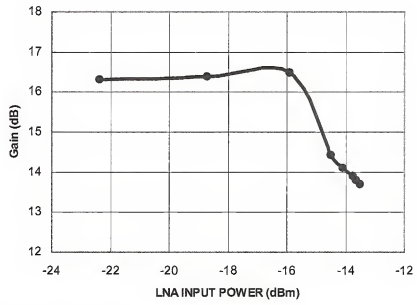


Figure 5-23. LNA linearity from embedded test

If the required noise figure is 2.0 dB and required available power gain is 15 dB, then estimated noise figure of the LNA under test can be obtained using equation 5-6. For example, at 5.0 GHz, the measured voltage gain is about 14 dB; hence the estimated noise figure is 2.4 dB, which is very close to the directly measured noise figure. If the tested LNA has a much higher noise figure with unacceptable value, this LNA is believed to be faulty.

5.5.5 Summary of the Proposed Test Scheme

With this arrangement of the proposed test scheme, the input examination of test high frequency test signal is overcome with the built-in wireless test signal source and the output examination of high frequency test response is overcome with the on-chip

detectors. With comparison, the conventional RF IC testing has to resort to costly high frequency probes to guarantee the integrity of high frequency input and output signals. For example, the probes used in the measurements of LNA in section 5.5.2 are at least several thousand dollars each, without mentioning the time spent on landing them to the chip under test.

Further, in the actual wafer test, it is difficult to input or output a radio-frequency signal to or from an integrated circuit in the form of a single chip, thereby allowing the inferior chips to be carried for further processing. Especially, in the case of multi-chip structure in which RF chip is contained in a package together with other base-band processing chips, if the inferior RF chip is subjected to further processing, the whole package containing the inferior chip becomes an inferior product. For this reason, the testing of RF chips at the stage of wafer state is becoming indispensable and the proposed test scheme make this kind of testing realizable. Therefore, the proposed test scheme can achieve cost reduction as well as an increase of the yield.

CHAPTER 6
SUMMARY AND FUTURE WORK

6.1 Summary

This work is focused on testing RF/Microwave circuit components at a lower cost compared to current RF/Microwave testing with expensive ATM systems. First, fundamental knowledge of describing embedded test is introduced. Second, several existing embedded test methods are investigated and a new wireless embedded test concept for RF/Microwave circuits is proposed. Then designs, simulation and measurement results of the necessary components for the proposed embedded test are discussed. These include an RF RMS detector, on-chip mini-antenna and CMOS frequency dividers. With an on-chip antenna and cascaded frequency dividers, a simple wireless RF/Microwave test source is designed, analyzed and the measurement results based on the fabricated chip are presented. Finally, an application of this wireless embedded test is described. The major contributions of this dissertation work are summarized as follows.

Based on the fundamentals of RF IC testing and existed embedded test methods, the conception of wireless embedded test for high-frequency circuits is proposed, which is mainly composed of an off-wafer (chip) tester plus test circuitry integrated with the DUT. The on-wafer (chip) test circuit receives a signal from the external signal source, modifies it into a suitable test stimulus to DUT, and then extracts the useful information from the response of the DUT into baseband signals, which are finally transmitted back

to the external tester. Some potential advantages include: direct connection between test source and circuit under test, parallel test of multiple chips, reliability and cost reduction.

A wide-bandwidth, high dynamic range, BiCMOS RF RMS detector based on the dynamic translinear principle is designed. The detector processes voltage signals at both input port and output port. Wide-bandwidth input and output circuits allow connecting voltage-mode signals to the internal current-mode circuitry. The internal current-domain circuit carries out the main computation. Auxiliary circuits are added to compensate for errors due to finite bipolar transistor gain. Measurements on a prototype chip demonstrate that the circuit is suitable for high frequency embedded on-chip testing.

On-chip mini-antenna is designed. Simulations with HFSS (EM simulator) and measurements on fabricated chip are demonstrated. Different types of high-speed frequency dividers are investigated, including both L-C injection-locked frequency dividers and flip-flop-based frequency dividers. The principle of injection locking based on Adler locking equation and nonlinear feedback loop is explained both mathematically and graphically.

A new topology of L-C injection-locked frequency divider is introduced. It stacks a PMOS-only L-C injection-locked frequency divider onto a NMOS-only L-C injection-locked frequency divider to form a fully differential injection-locked frequency divider. Compared with the existed fully differential injection-locked frequency dividers, this stacked topology has higher injection efficiency and input sensitivity.

Multi-tone performance of injection-locked frequency dividers is investigated. The theoretical analysis shows that only the strongest input tone can be divided directly to the output and the rest of input tones do not have corresponding divided tones shown at the

output. However, the input beat frequency, which is defined as the frequency difference between two input signals, is carried out to the output without any changes. Thus, besides the direct divided strongest input tone, the other output components are spaced evenly from this tone by the same input beat frequency. Measurement results on the fabricated injection-locked frequency divider verify the validity of the above theoretical analysis.

A new built-in RF/Microwave signal source with wireless operation is developed. The components inside this signal source are an on-chip mini-antenna, frequency dividers and buffers. With wireless communications between on-chip antennas and an off-chip antenna, the external signals are transferred onto the chip where the receiver antenna is located. The received signals of very high frequency are divided by frequency dividers to the operation frequency of circuit under test. The buffer functions as the interface between the core of the built-in source and the rest circuits. As an example, a 20 GHz built-in signal source with two-stage frequency divider is discussed in detail. Both of simulation and measured performance of this source are presented.

The proposed built-in test signal source and on-chip detectors are applied to an embedded test scheme for a 5 GHz LNA. With correct post-processing of measured data, the performance parameters obtained from the proposed embedded test scheme can accurately track those obtained from conventional measurements. Within the measurable frequency range, the differences of the measured voltage gain are less than +/- 1 dB.

6.2 Future Work

Embedded test for RF IC is still a topic of active research. Issues such as area consumption, reliability, calibration, cost and yield continue to intrigue researchers.

Within the conception of the proposed wireless embedded test, a few possible future works are suggested.

The improvements on on-chip detectors could be focused on the the replacement of bipolar detector with CMOS detector. In these days, with the scaling of CMOS technology, the analog performance of MOS transistor is improved. From the point of cost and low power, MOS technologies are becoming dominant not only in the area of digital integrated circuits but also in the area of analog integrated circuits. Hence, it will be much useful to implement a MOS-only embedded test scheme rather than BiCMOS embedded test scheme. Since in the proposed wireless embedded test scheme the only component made of bipolar transistors is the detector, it is important to find a new design to implement a high-speed CMOS detector.

In addition, it is advisable to design an on-chip detector which is capable of detecting both amplitude and phase information of the signal. One possible way to implement such a detector could be that based on multipliers.

As for the built-in wireless test signal source, it is desirable to further decrease its size. By transmitting higher frequency signal onto the chip, it is possible to smaller on-chip antenna. On the other hand, it is possible to explore other structures of on-chip antenna to further increase antenna gain and efficiency at the same size or improve the input sensitivity of the frequency divider. For instance, it is possible to build an on-chip antenna with a whole specified top metal. Thus the horizontal chip area can be reused at the price of an additional metal layer. Certainly, the cost and the effect of this antenna made of the additional metal layer need to be examined carefully. Alternatively,

frequency dividers with better input sensitivity and smaller area consumption should be investigated as well.

The proposed embedded test scheme for LNA with the wireless test source and detectors need to be further studied and possible implementations are worth to be further investigated. One possible improvement is to add on-chip RF switches as shown in figure 6-1. In this way, field tests of the chip become possible with turning on or off these on-chip switches. The challenges are the performance of CMOS switches at such high frequencies.

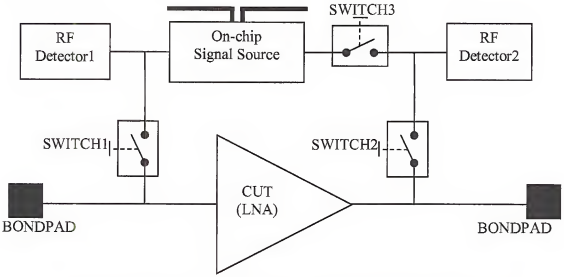


Figure 6-1. One possible implementation of wireless embedded test scheme for LNA.

As far as the chip area occupied by embedded test circuits is concerned, the present embedded test scheme is particularly suitable for testing of small-lot production or inefficient production, in terms of its easy estimation in the wafer state and cost reduction due to omission of the external devices. With the further decrease of the size of embedded test circuits, it is possible to move this embedded test to large-lot production.

In this dissertation, only low noise amplifier is employed to demonstrate the application of the proposed wireless embedded test vehicle. More applications of this wireless embedded test vehicle can be explored in the future.

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